VXI Rubidium

MODEL 3352

PUBLICATION NO. 980900

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RETURN of PRODUCT

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an auto-transformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

Racal Instruments

CE Declaration of Conformity

We

Racal Instruments Inc.
4 Goodyear Street
Irvine, CA 92618

declare under sole responsibility that the

3352-GPS VXI RUBIDIUM , P/N 407919, -001, -002
conforms to the following Product Specifications:

EMC: EN61326:1998 +A1: 1998 +A2: 2001

FCC CFR 47, PART 18 SUBPART B **CLASS A**

ICES-003 ISSUE 4: February 2004 **CLASS A**

Supplementary Information:

The above specifications are met when the product is installed in a Racal Instruments certified mainframe with faceplates installed over all unused slots, as applicable.

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (modified by 93/68/EEC).

Irvine, CA, April 13, 2005

VP of Engineering
Karen Evensen

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Chapter 1
INTRODUCTION

General Description

The Racal Instruments' Model 3352 is a single-slot C-size VXI module that provides a GPS disciplined 10MHz Rubidium frequency standard. The module provides two 1V rms sinewave and eight TTL level outputs. The GPS timing receiver is capable of tracking up to 12 satellites and includes automatic site survey for accurate antenna position location. An external power input keeps the Rubidium very stable over time and keeps the GPS settings in memory from becoming corrupt during the absence of VXI test station power.

Using ANSI Standard M-module building blocks, the 3352 integrates a Rubidium oscillator, a GPS timing receiver, and clock and trigger distribution into a single slot package. The module is an integration of several standard products as shown below. The M210 Trigger Distribution board and GPS antenna are optional. The GPS antenna option includes a Motorola Oncore Timing2000 antenna and 15 meters of coaxial cable.

Product Configuration

The 3352 comes in four different configurations. The versions are differentiated by the amount of M-module population. The following lists the different versions of the 3352 along with a table of M-module population for each.

1.) 407919 3352 with GPS
2.) 407919-001 3352 w/o GPS
3.) 407919-002 3352 with GPS and Trigger Distribution (RTCASS version)
4.) 407919-003 3352 with Digital I/O. w/o GPS

3352 Version	VX405C	M212	M213	M1708	M210	M1714
407919	X	X	X	X		
407919-001	X	X		X		
407919-002	X	X	X	X	X	
407919-003	X	X		X		X

This manual covers all four versions of the 3352. For a version that does not have a particular M-module associated with it, skip the corresponding section in the manual.

MTBF

The following is the MTBF calculations for each of the modules that make up the 3352 followed by the MTBF for each 3352 version. The MTBF was obtained using the Relex 7.1.2 software with calculations configured for MIL-HDBK-217 FN2 as the model and Method 1 Case 3 for calculation method.

1.) VX405C Carrier	62,622 hrs
2.) M1708	150,000 hrs
3.) M210	199,508 hrs
4.) M213	
a.) M213 board	264,879 hrs
b.) M12 GPS receiver	1,600,1000 hrs
5.) M212	
a.) M212 board	926,476 hrs
b.) Rubidium Module	174,720 hrs
6.) M1714	765,387 hrs

The following is the calculated values for each of the 3352 variants:

1.) 3352 w/ GPS training (407919)	29,551 hrs
2.) 3352 w/o GPS training (407919-001)	33,967 hrs
3.) 3352 w/ GPS training and PG dist(407919-002)	25,740 hrs

Programming

A VXI*plug&play* driver is available that provides high level functions to configure, operate and get status of the 3352. The driver includes an interactive soft front panel application that allows the user to interactively control the 3352 from any Windows based VXI host. Also included are 32-bit Windows DLL and LIB files that allow the user to call the VXI Plug and Play driver from almost any programming environment including: C, C++, Visual Basic, LabWindows/CVI, and LabView. The driver is provided with source code as well as help files to assist the developer with programming the module.

Various minimum system requirements must be met for use of the VXI*plug&play* driver. These minimum requirements are specified in the VXI Plug and Play specification document VPP-2. In general, the minimum hardware requirements for the Windows framework are:

- Must be 100% IBM PC compatible
- Must have an 80486/33 MHz or greater CPU with floating point
- Must have at least a 120-MB hard disk

- Must have a VGA or higher compatible monitor
- Must have at least 8-MB RAM (Racal Instruments recommends 16-MB)
- Must have a Windows compatible mouse
- Must have the capability to control a VXI system

In addition, the following are minimum software requirements must also be met:

- Microsoft Windows 95, 98, ME, NT, 2000, XP or higher
- VISA I/O Library Version 2.0 of higher (most recent version is recommended)
- Minimum VXI Resource Manager software needed to configure a VXI system

To install the VXI*plug&play* driver, run *Setup.exe* from the installation disks or from the downloaded files. Follow the instructions on the installation wizard to complete the installation. The recommended installation directory is the system VXIpnp directory. The driver files will be installed on your system as follows:

File	Directory	Description
ri3352_32.dll	VXIpnp\WinNT\bin	32-bit Windows DLL
ri3352.lib	VXIpnp\WinNT\lib\bc	Borland compatible C library
ri3352.lib	VXIpnp\WinNT\lib\msc	Microsoft compatible C library
ri3352.h	VXIpnp\WinNT\include	ANSI C header file
ri3352.exe	VXIpnp\WinNT\ri3352	Soft front panel Executable
ri3352.c	VXIpnp\WinNT\ri3352	Driver source code
ri3352sfp.c	VXIpnp\WinNT\ri3352	Soft front panel source code
ri3352.fp	VXIpnp\WinNT\ri3352	LabWindows\CVI interactive function panels
ri3352.doc	VXIpnp\WinNT\ri3352	Driver documentation
ri3352.hlp	VXIpnp\WinNT\ri3352	Driver help file
ri3352sfp_help.hlp	VXIpnp\WinNT\ri3352	Soft front panel help file
ri3352uir.uir	VXIpnp\WinNT\ri3352	Soft front panel user interface file for LabWindows/CVI
ri3352uir.h	VXIpnp\WinNT\ri3352	Header file for the soft front panel user interface

For details on the specific driver functions or on operating the soft front panel application, refer to the installed help files. If low-level (i.e. register level) programming details are needed for any of the modules that make up the 3352 (M212, M213, M1708, M210, M1714), refer to documentation for the specific module, which is contained in separate chapters of this manual.

The 3352 requests four VXI logical addresses from the resource manager. Each logical address refers to one of the four modules that make up the integrated unit. When accessing the VXI Plug and Play driver, only the base address (position A of the VX405C) should be used.

NOTE: The M210 Trigger Distribution Module is configured with the input thresholds set to fixed factory default levels. No programming is required for this module and thus the software driver does not refer to it.

Chapter 2
VX405

General Description

The VX405C is a single slot, register-based, C-size, VXIbus compatible carrier module that provides electrical and mechanical support for up to six single M or MA modules (M/MAs). Of these six M modules connections, four are used for a fully populated 3352. This is because the M210, M1714 and the M212 are double wide M modules and only one of the two connections is enabled. The connections that are enabled are A, C, D and E for a fully populated 3352. Each installed M/MA module appears as an independent VXI instrument to the VXI resource manager. Full VXI and MA-Module triggering and addressing is supported.

Purpose of Equipment

This module provides a carrier function for the plug-in modules that make up the 3352 Rubidium system.

Specifications of Equipment

Key Features

- Supports up to six (6) ANSI/VITA 12-1996 compliant single wide M or MA-modules, or any valid combination of 2, 3, or 4 wide modules
- Supports extended M-Module functions (MA) such as extended 24-bit addressing for up to 16 Mbytes of memory, 32-bit data bus, and trigger signals for synchronization of MA-Modules
- VXI A16, A24 and A32 addressing supported
- D8, D16, and D32 accesses supported
- Individual Logical Addressing of M/MA-modules
- Isolated, filtered, and fused +5V, +12V, and -12V supplies for each M-module
- ±24V Auxiliary Power Connector (Rev. C or higher assemblies only)
- Separate Software Programmable Interrupt Levels
- MA-Module TRIGA and TRIGB can be connected to any VXI TTL Trigger Line through software control

- M/MA Module data access time < 800ns
- Front panel EMI shielding
- Interactive Mezzanine Control software available

Electrical

The VX405C only requires the +5V power from the VXI back plane; however, ±12V may be required by installed M-modules and ±24V may be required if the auxiliary power connection is used. The carrier's peak module current (I_{PM}) for the +5V supply is 1.2 amps. A total of 7.2A of +5V is available for the VXI backplane.

For electrical information on individual M/MA's, please reference each M/MA's documentation. The power requirements for each M/MA installed must be added to the VX405C's requirements for the total module's requirements.

	-0001		-0002
	Power off resetting fuses		Standard replaceable fuses
	Hold Current	Trip Current	
Total Max. Current +5V	5A	10A	10A
Total Max. Current +12V	2.5A	5A	
Total Max. Current +12V	2.5A	5A	

	+5V	+12V	-12V	+24V	-24V
Total Available from VXI Slot	7.2A	1.0A	1.0A	1.0A	1.0A
Used by VX405C internal logic	1.2A	0A	0A	0A	0A
-0001 fused level	5.0A	2.5A	2.5A	1A	1A
-0002 fused level	5.0A	2.5A	2.5A	1A	1A

	+5V	+12V	-12V
Allowed by specification per M-Module position	1A	0.2A	0.2A
-0001 fused level per position	1.25A	0.3A	0.3A
-0002 fused level per position	2A	1A	1A

Mechanical

The mechanical dimensions of the module are in conformance with the VXIbus specification Rev. 1.4 for single slot 'C' size modules. The nominal dimensions are 233.35 mm (9.187 in) high x 340 mm (13.386 in) deep.

Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +55°C
Storage Temperature:	-40°C to +75°C
Humidity:	<95% without condensation

Installed M/MAs may differ in environmental specification. Refer to each individual M/MA's documentation for information.

Bus Compliance

The module complies with the VXIbus Specification Revision 1.4 for C-size register based modules and with VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821.

Manufacturer ID:	FC1$_{16}$ or VXI-IDENT value
Model Code:	FF2$_{16}$ or VXI-IDENT value
VXI Access Type:	Register Based
VXI Addressing:	A16/A24/A32
VXI Data Transfer:	D8/D16/D32
VXI Sysfail:	supported
VXI Interrupts:	ROAK or RORA, programmable levels
VXI Local Bus:	not used
TTL Triggers:	SYNC trigger protocol supported
Memory Requirements:	M/MA dependent, up to 16Mbytes (VXI 32Mbytes)
M/MA-Module Compliance: A24,	M-Module, MA-Module, A08, D08, D16, D32, INTA, INTB, INTC, TRIGI, TRIGO, IDENT

Applicable Documents

ANSI/VITA 12-1996American

National Standard for The Mezzanine Concept
M-Module Specification, Approved May 20, 1997
VMEbus International Trade Association
7825 E. Gelding Dr. Suite 104
Scottsdale, AZ 85260-3415
E-mail: info@vita.com URL: http:\www.vita.com

Installation

Unpacking and Inspection

Verify that there has been no damage to the shipping container. If damage exists, retain the container, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to RACAL INSTRUMENTS. If there is no damage to the shipping container, carefully remove the module from its box and anti-static bag and inspect for any signs of physical damage. If damage exists, report immediately to RACAL INSTRUMENTS.

Handling Precautions

The VX405C (3352) contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

Installation of M\MA Modules

M/MA modules must be installed before the VX405C (3352) is installed into the VXI system. To install modules, remove the VX405C's top shield and front panel covers as needed. ***There is never a need to remove the VX405C's bottom shield.*** Install M/MAs by firmly pressing the connector on the M/MA together with the connector on the carrier. Secure the M/MA through the holes in the bottom shield using screws provided with the M/MA. For installing M/MA modules in locations E or F, longer screws are provided (if necessary) to accommodate the standoffs required on the VX405C in those locations.

WARNING: The VX405C supports MA-Modules that use three row interface connectors. M-Modules use only two rows connectors and must be correctly positioned to use rows A and B on the carrier. When using M-Modules, row C on the VX405C is left unconnected.

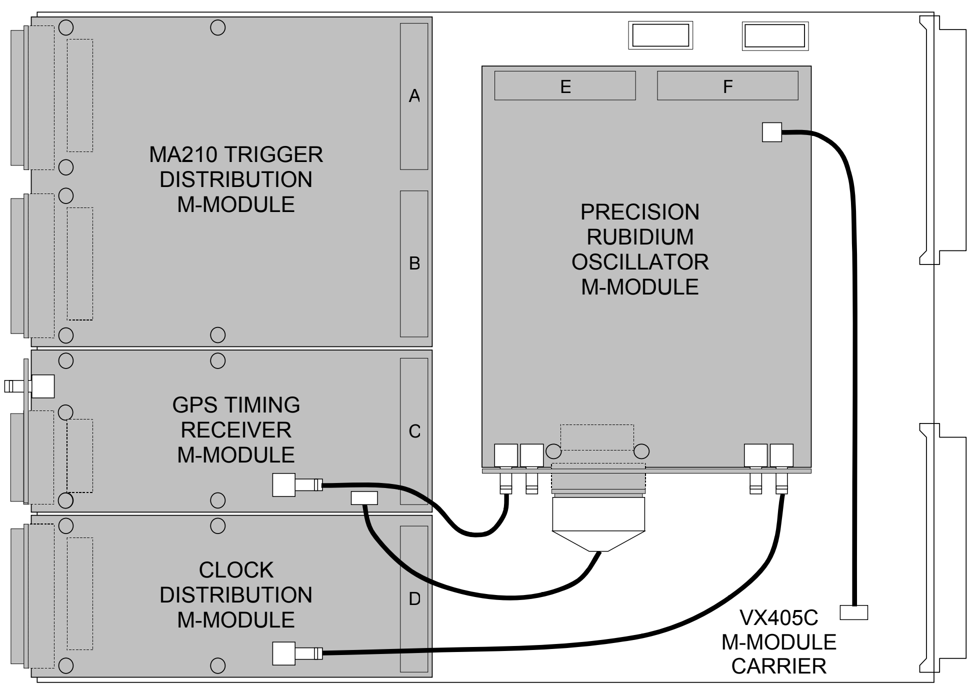


Figure 2-1 3352 M/MA Configuration Diagram

Installation of VX405C Carrier (3352)

Set the module's logical address and addressing mode as described in Chapter 2 sections Logical Address Selection and Address Space Selection. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Chapter 2 section Operating Instructions.

Preparation for Reshipment

1. Use the original packing material when returning the switching module to Racal Instruments for servicing. The original shipping carton and the instrument's plastic foam will provide the necessary support for safe reshipment.

2. If the original packing material is unavailable, wrap the switching module in an ESD Shielding bag and use plastic spray foam to surround and protect the instrument. Reship in either the original or a new shipping carton.

Functional Description

General

The VX405C carrier provides a mechanical and electrical interface between a VXIbus system and up to six ANSI/VITA 12-1996 standard M/MA modules. The carrier provides VXI register configuration and access to the M/MA module's I/O Space and Memory (if present). Each M/MA is controlled separately and appears as a different logical address in the VXI environment. A simplified block diagram of the module is shown in **Figure 2-2**. The VX405C has no logical address or programmable registers associated with it, thus allowing the carrier to be completely transparent in the VXI system.

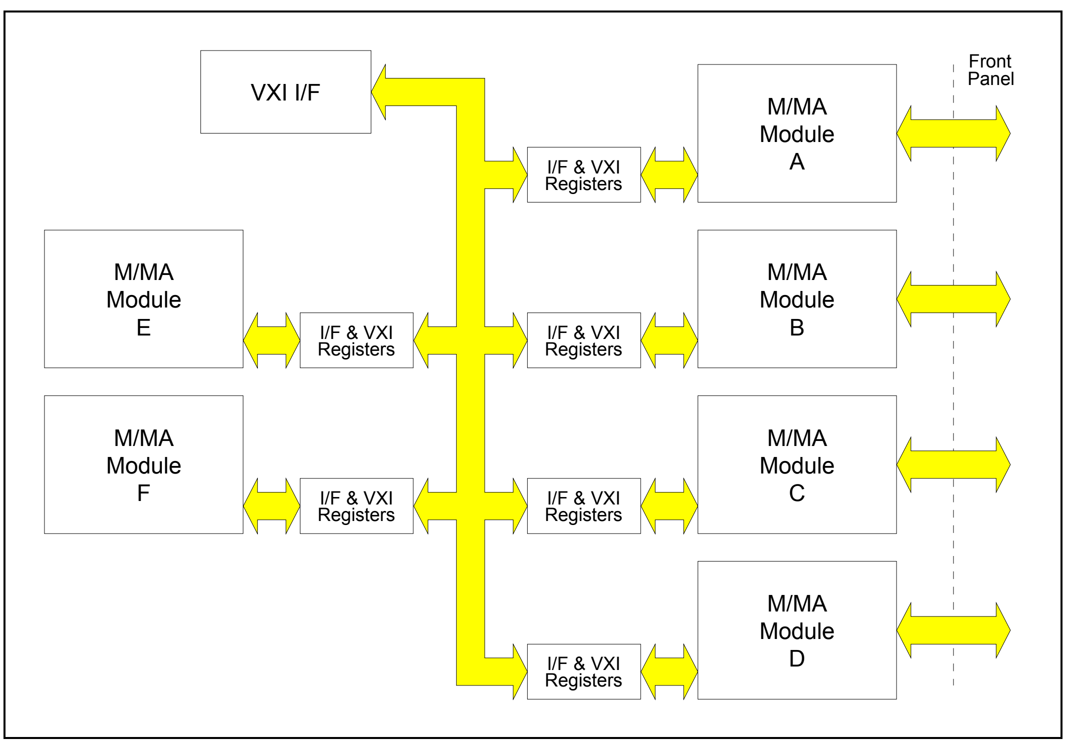


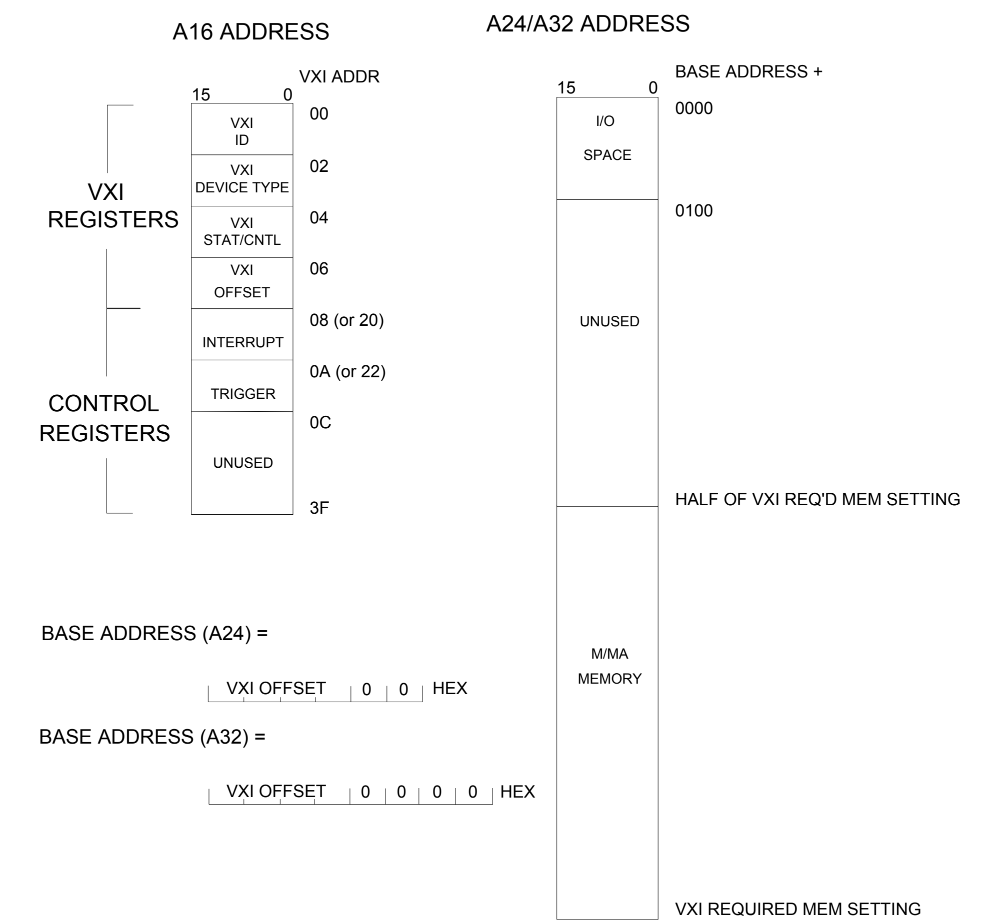
Figure 2-2 VX405C Functional Block Diagram

Interfaces

The six M/MA locations interface electrically and mechanically with industry standard M/MA modules meeting the ANSI/VITA 12-1996 M-Module Specification (approved May 20, 1997). Each M/MA has its own I/O connector and is accessible through the front panel of the VX405C via the connector or a user provided cable.

I/O and Memory Addressing

The VX405C supports D8 (Even/Odd), D16, and D32 data access as well as A16, A24, and A32 addressing. The VXI registers of the M/MAs are accessible in the A16 address space. The VXI Offset Register is used to map the M/MA I/O Space and MA Memory (if applicable) into the A24 or A32 addressing space. For MA's that support memory, the memory begins at the mid-point of the total memory required as shown in **Figure 2-3**.



Notes:
1) Refer to VXI Device register (02) for details on Req'd Memory Setting
2) AAA bit of the VXI STAT/CNTL register must set to a '1' to access memory or I/O space.
3) Byte Addressing is referenced above.

Figure 2-3 Memory Organization

Triggers

Each M/MA is allowed two trigger lines, TRIGA and TRIGB. Triggers may be input or output. The VX405C Carrier provides software programmable connection to any VXI TTL Trigger line (SYNC Protocol). Each M/MA trigger can be enabled, logically inverted, configured as input or output, and mapped to any of the eight VXI TTL Trigger lines.

Interrupts

Each M/MA can support one interrupt request as specified in the ANSI/VITA 12-1996 Specification. Each interrupt can be programmed to an individual interrupt level and is handled separately during interrupt acknowledge cycles. A hardware priority for each interrupt programmed to the same level, begins with M/MA slot A's interrupt being the highest priority and M/MA slot F's Interrupt being the lowest priority. For further detail, refer to Chapter 2 section Interrupts (below).

Hardware Configuration

The logical address, address space, and positions of the occupied M/MA-module locations must be configured prior to installing the carrier into the chassis. The configuration is done using the switches described below and shown in **Figure 2-4**.

Logical Address

Each M/MA location has its own logical address based on a five position address switch. The selected logical address establishes the address for position A. The other positions follow in sequential or modulo-8 order, depending on the Modulo Select switch. See Chapter 2 section Logical Address Selection for more details.

Modulo Select

This switch allows the user to set the desired numbering (sequential or modulo-8) of the logical addresses assigned to each M/MA location on the VX405C. The switch is located at position 7 of the logical address switch. For further details, refer to Chapter 2 section Logical Address Selection.

Address Space

This switch selects either A24 or A32 addressing. The switch is located at position 8 of the logical address switch. For A24 addressing the switch should be set in the OPEN or '1' position.

M/MA Module Enable

Six switches are provided to enable the individual M/MA locations. Each switch corresponds to an M/MA location and must be enabled before the carrier will recognize an M/MA present. The following is the switch settings for each of the 3352 configurations.

SW2-1 thru 6	A	B	C	D	E	F
FOR **P/N: 407919**	DIS	DIS	EN	EN	EN	DIS
FOR **P/N: 407919-001**	DIS	DIS	DIS	EN	EN	DIS
FOR **P/N: 407919-002**	EN	DIS	EN	EN	EN	DIS

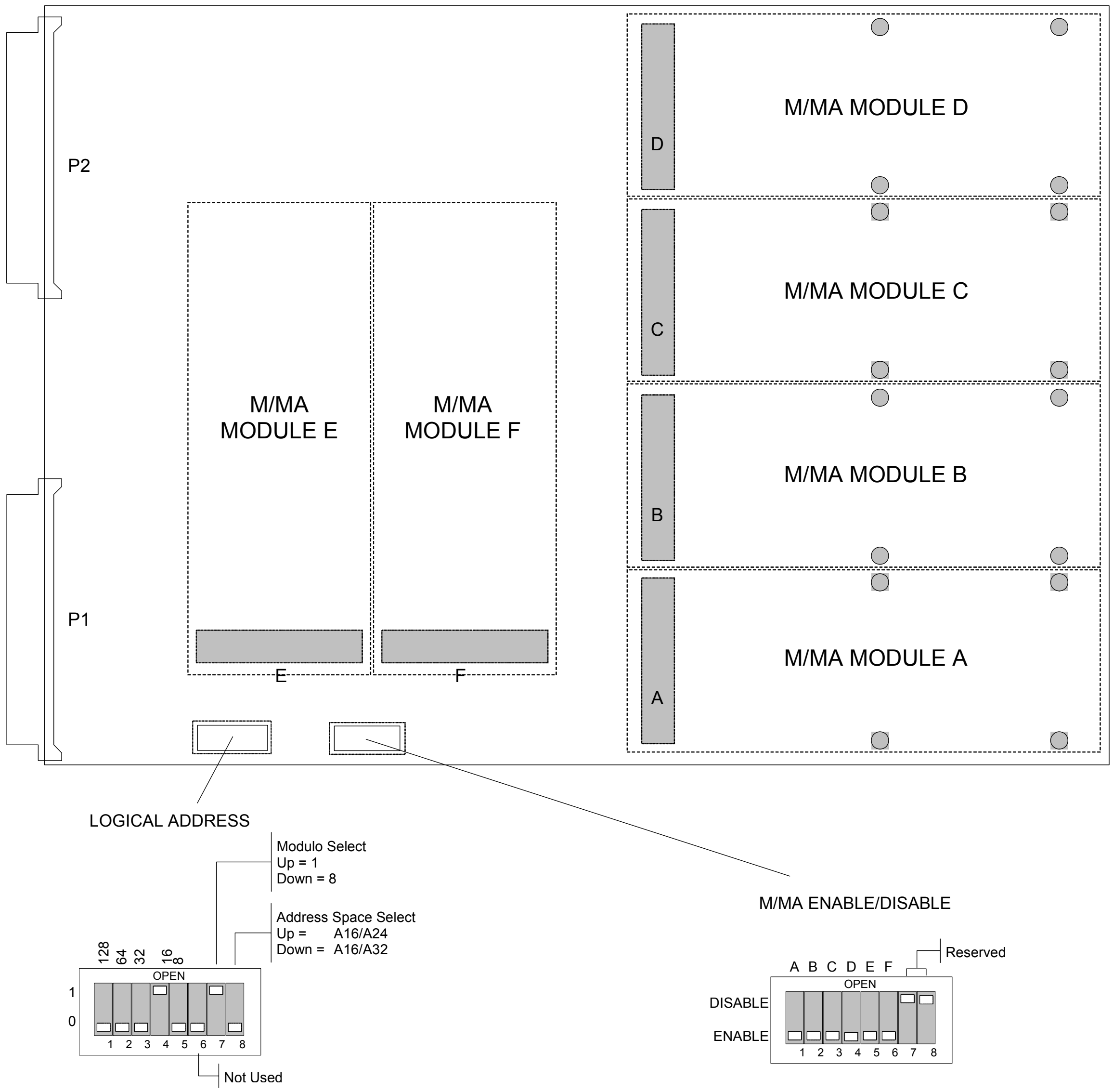


Figure 2-4 VX405C Hardware Configurable Controls

Indicators

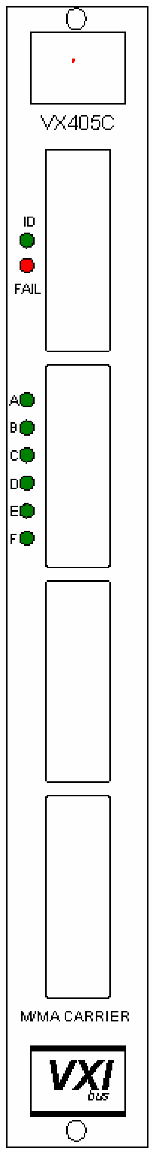
Eight LED indicators are provided on the front panel. Their functions are:

FAIL: This front panel LED indicates the PASS/FAIL (SYSFAIL) status. The LED illuminates during reset, initialization, or if there is a failure on the VX405C Carrier itself.

ID: This front panel LED illuminates whenever the host processor applies the MODID signal to the slot the module is occupying.

A, B, C, D, E, F: These front panel LEDs illuminate whenever that M/MA is properly accessed by the host processor.

Connectors



Front Panel Connector

The front panel connectors come directly from the M/MAs them-selves, therefore they are M/MA dependent. Front panel covers are provided to close front panel openings on any unused M/MA locations. The covers should be used to control airflow and EMI leakage when there is no M/MA module installed.

Rear Connectors

The P1 and P2 connectors are configured in accordance with the VXI specification. (See **Figure 2-5**)

Figure 2-5 3352
Front Panel

Configuration Registers

There are a variety of registers used to configure and control the VX405C module. The VXI configuration registers provide for control and status as required by the VXIbus specification. An address map of the registers is shown in **Table 2-1.**

Table 2-1 VXI Register Address Map

A16 Address	Register Description
Base + 00	VXI ID
Base + 02	VXI Device Type
Base + 04	VXI Status/Control
Base + 06	VXI Offset Register
Base + 08 (or 20)	Interrupt Control Register
Base + 0A (or 22)	Trigger Control Register

VXI Configuration Registers

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in **Figure 2-6**.

VXI Identification (ID) Register

($Base + 00_{16}$) This read-only register provides the manufacturer identification, device classification (i.e., register based), and the addressing mode (i.e. A32).

VXI Device Type Register

($Base + 02_{16}$) This read/write register provides the model code (see note) identifier and allows the user to set the M/MA's required memory.

> NOTE: The manufacturer and model code identification depends on the installed M/MA-Module's support of the VXI extension to the optional M-Module IDENT function. For modules that support the VXI IDENT extension (non-standard), the manufacturer and model code of the M/MA-Module is reported and the required memory is automatically set according to the M/MA-Module requirements. For all other modules, C & H Technologies ($FC1_{16}$) is reported as the manufacturer and the VX405C ($FF2_{16}$) as the model code. Additionally, the user may have to set the required memory. Refer to M/MA Module Identification for details on the VXI INDENT Extension

VXI Status/Control Register

(Base + 04_{16}) A read of this register provides the state of the P2 MODID* line and the SYSFAIL inhibit, ready and self-test status. A write to this register allows disabling of the SYSFAIL function and individual reset of the associated M/MA module.

VXI Offset Register

(Base + 06_{16}) This read/write register controls the offset value for addressing the M/MA I/O space and memory. The VXI system resource manager or control module sets this value according to the memory requirements specified for this module and the memory requirements of the other instruments in the system.

00 **VXI ID**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	Device Class		Address Space		Manufacturer ID											

Device Class ⇨ Device Class (11 = Register Based)
Address Space ⇨ Address Space (00 = A16/A24, 01 = A16/A32, 10 = reserved, 11 = A16 Only)
Manuf. ID ⇨ Manufacturer Identification (see text for details)

02 **VXI Device Type**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Required Memory															
Read	Required Memory				Model Code											

Model Code ⇨ Model code (see text for details)
Required Memory ⇨ Required memory (value depends on memory required by M/MA module and VXI address space setting, see table below)

Mem Rq'd by M/MA	A32 Address Space	A24 Address Space
0 bytes	F (64K)	E (512 bytes)
128 bytes	F (64K)	E (512 bytes)
256 bytes	F (64K)	E (512 bytes)
512 bytes	F (64K)	D (1K)
1K	F (64K)	C (2K)
2K	F (64K)	B (4K)
4K	F (64K)	A (8K)
8K	F (64K)	9 (16K)
16K	F (64K)	8 (32K)
32K	F (64K)	7 (64K)
64K	E (128K)	6 (128K)
128K	D (256K)	5 (256K)
256K	C (512K)	4 (512K)
512K	B (1M)	3 (1M)
1M	A (2M)	2 (2M)
2M	9 (4M)	1 (4M)
4M	8 (8M)	0 (8M)
8M	7 (16M)	-
16M	6 (32M)	-

Figure 2-6 VXI Configuration Registers

04 **VXI Status/Control**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	AAA	-	-	1	1	1	1	1	1	1	1	1	-	-	SI	RST
Read	AAA	MID	CSE	1	1	1	1	1	1	1	1	1	RDY	Pass	0	0

AAA ⇨A24/A32 Access (0 = disabled)
MID ⇨Module ID Status (0 = P2 MODID* line is selected)
CSE ⇨Check Sum Error. (0 = error reading non-volatile memory during power-up. Reset on read, 1 = OK)
RDY ⇨Ready (1 = ready)
Pass ⇨Pass/fail indicator (0 = executing or failed, 1 = passed)
SI ⇨Sysfail Inhibit (1 = inhibit, see note)
RST ⇨Reset (writing a '1' to this bit resets the M module; after a minimum of 100 μs a '0' must be written to resume normal operation)

Note: The Sysfail Inhibit is a VXI slot inhibit; therefore setting the inhibit bit on any M/MA module will inhibit SYSFAIL on all M/MA modules.

06 **VXI Offset Register**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Offset Value															
Read	Offset Value															

Offset Value⇨Offset to M/MA's I/O Space and Memory (if applicable)

Figure 2-6 VXI Configuration Registers (continued)

Special Function Register

Interrupt Control Registers (base + 08_{16} or base + 20_{16}) This read/write register sets the interrupt level, and provides the upper byte of vector for M/MA interrupt types INTA and INTB.

Trigger Control Register (base + $0A_{16}$ or base + 22_{16}) This read/write register selects a VXI TTL Trigger line for the TRIGA and TRIGB functions, and sets them as input or output using the VXI TTLTRG Synchronous (SYNC) Trigger Protocol.

08

Interrupt Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Interrupt Vector								-	-	-	IT	IVE	Interrupt Level		
Read	Interrupt Vector								-	-	-	IT	IVE	Interrupt Level		

Interrupt Vector⇨ Upper 8 bits of the interrupt vector for type INTA and INTB interrupts. Default = 0.
IT⇨ Interrupt Type (0 = follows interrupt type used by installed M-Module, 1 = ROAK regardless of M-Module interrupt type)
Interrupt Level⇨ Interrupt Level for the M/MA interrupt. Level of '0' disables the interrupt. Default = disabled.
IVE⇨Interrupt vector enable (0 = returns the M-module vector (if supported by the M-Module), 1 = returns the interrupt vector programmed in this register). Default = 1.

0A

Trigger Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	BEN	BDIR	BINV	-	-	Trig B TTL Sel			AEN	ADIR	AINV	-	-	Trig A TTL Sel		
Read	BEN	BDIR	BINV	-	-	Trig B TTL Sel			AEN	ADIR	AINV	-	-	Trig A TTL Sel		

AEN ⇨ Trigger enable for Trig A (1 = enable, 0= disable). Default = disable.
ADIR ⇨ Trigger direction for Trig A (0 = input (VXI to M-Module), 1 = output (M-Module to VXI)). Default = input.
AINV ⇨ Trig A invert bit. (1 = invert logical level of input or output trigger A). Default = 0, non-inverting.
Trig A TTL Sel ⇨ Trigger A Mapping to VXI TTL Trigger lines 0 -7. Default = 0.
BEN ⇨ Trigger enable for Trig B (1 = enable, 0= disable). Default = disable.
BDIR ⇨ Trigger direction for Trig B (0 = input (VXI to M-Module), 1 = output (M-Module to VXI)). Default = input.
BINV ⇨ Trig B invert bit. (1 = invert logical level of input or output trigger B). Default = 0, non-inverting.
Trig B TTL Sel ⇨ Trigger B Mapping to VXI TTL Trigger lines 0 -7. Default = 0.

Figure 2-7 Special Function Registers

Operating Instructions

General

The VX405C (3352) is configured through a series of hardware switches and software controlled registers as below. The switches enable the M/MA slots and configure the logical addresses of the M/MAs. The VX405C has software controlled registers for each module. These registers provide configuration of interrupts, triggers, A24/A32 addressing, and required memory. All other M/MA controls are dependent on a specific M/MA and reside on that module (in I/O and memory space).

Hardware Configuration

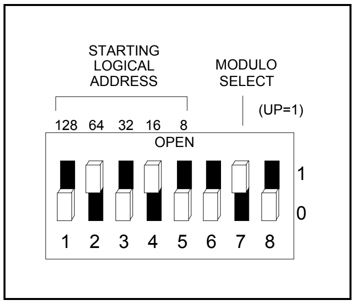
> **CAUTION: All hardware configurations must be done only while the power to the module is OFF.**

Logical Address Selection

The logical address is set for each M/MA module by selecting the starting logical address and the desired sequencing (sequential or multiple of 8) of addressing using the toggle switches provided on the carrier. With sequential logical addressing (Modulo Select switch in the Up position), the starting logical address can be selected as any multiple of 8 (i.e., 8, 16, ..., or 248). The M/MA in location A is assigned the starting logical address and the remaining locations (enabled or disabled) are assigned logical addresses in sequential order (i.e., 8, 9, 10, etc.). With Modulo-8 logical addressing (Modulo Select switch in the Down position), the starting logical address can be selected as any multiple of 64 (i.e., 64, 128, or 192). The M/MA in location A is assigned the starting logical address and the remaining locations (enable or disabled) are assigned logical addresses in multiples of eight (i.e., 64, 72, 80, etc.). A disabled M/MA location is still counted when determining the logical address of the enabled locations; however, the disabled location will not respond when queried by the resource manager and the logical address can be used elsewhere in the system.

Care should be taken to ensure that none of the modules have the same logical address as another module in the VXI system. Position 1 on the switch is the most significant bit and has a weighted value of 128 when the switch is in the OPEN position. Position 5 on the switch is the least significant bit and has a weighted value of 8 when the switch is in the OPEN position. It is important to note that if the modulo select switch is set to ‘8’ (the DOWN position), only logical address switch settings of 64, 128, 192 are valid. The sum of the weighted values of all the switches in the OPEN position, along with the values in the table below, give the M/MAs' logical address.

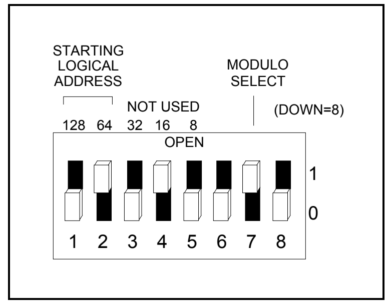
Example of sequential addressing:



With the above switch settings, the starting logical address is 64 + 16 = 80 and the logical addresses would be assigned as follows:

M/MA Location	Location Enabled	Assigned Logical Address
A	Yes	80
B	Yes	81
C	Yes	82
D	No	unassigned
E	No	unassigned
F	Yes	85

Example of Modulo-8 addressing:



With the above switch settings, the starting logical address is 64 and the logical addresses would be assigned as follows:

M/MA Location	Location Enabled	Assigned Logical Address
A	Yes	64
B	Yes	72
C	Yes	80
D	No	unassigned
E	No	unassigned
F	Yes	104

Address Space Selection

A single switch is provided that selects either VXI A16/A24 or A16/A32 addressing for the entire carrier. This switch is located in position 8 of the logical address switch. The UP (OPEN) position of this switch corresponds to A16/A24 and the DOWN position to A16/A32.

M/MA Module Enable

Six switches are provided to enable the individual M/MA locations. Each switch represents an M/MA location and must be enabled before the carrier will recognize a module as present. These switches are positions 1 - 6 of the M/MA switch and correspond to M/MA locations A - F respectively. With the switch in the UP (OPEN) position, the M/MA in that location is disabled. Conversely, with the switch is in the DOWN position, the M/MA in that location is enabled. ***Switch positions 7 & 8 are reserved for test purposes and must be in the DOWN position for normal operation.***

Software Configuration

Required Memory Setting

The amount of memory space allocated for a module by the system resource manager or control module is specified in the Required Memory field of the VXI Device Type register (0x04). The default Required Memory setting is the minimum amount allowed by the VXI address space selected. A24 addressing allows a minimum of 512 bytes and A32 addressing allows a minimum of 64Kbytes.

> NOTE: In order to access the M/MA-Module IO Space and memory, the AAA bit in the VXI Status/Control register (0x04) must be set high. This is usually done by the resource manager after allocating memory.

For M-Modules that have only IO Space (256 bytes), the default Required Memory setting is sufficient and no changes to this field are required.

For MA-Modules that have on-board memory, the Required Memory field must be changed to cause the resource manager to allocate enough memory space for the IO Space and memory contained on the MA-Module. Since the VX405C maps a MA-Module's IO Space into the lowers 256 bytes of the allocated memory space and the MA-Module's memory into the upper half of the allocated memory space, the VXI Required Memory must be set to twice the MA-Modules required memory.

For example, if an MA-Module has 512Kbytes of on-board memory, then 1Mbyte of VXI memory space must be allocated. The modules 256 bytes of IO Space is mapped starting at the *Offset* + 0x000000 (A24) and the 512Kbytes of memory begins at the *Offset* + 0x080000 (A24). Proper settings are given in the table provided under the VXI Device Type register description in **Figure 2-6**.

To change the Require Memory field, simply write the new value to VXI Device Type register. The Model Code bits are ignored. The new setting is stored in non-volatile memory and will remain the set value until it is changed again. When the required memory bits are written, the VX405C must be **powered off** and a resource manager re-ran before the change will take effect. *Due to the required memory setting being stored in non-volatile memory, a short amount of time is required before the VXI Device Type Register can be accessed again after a write. During this time, the VXI Ready Bit is cleared in the VXI Status/Control Register (0x04), and then set back to '1' when access to the VXI Device Type Register is permitted.*

NOTE: If the installed M/MA-Module supports the VXI IDENT extension (non-standard) to the optional M-Module IDENT function, the required memory is automatically set according to the M/MA-Module requirements. Refer to M/MA Module Identification for details on the VXI IDENT Extension.

Triggers

If the TRIGI or TRIGO functions are supported by an M/MA, any of the eight VXI TTL Trigger lines can be connected as either an input or output to TRIGA or TRIGB of the M/MA. A software programmable register (0x0A or 0x22) is provided for each M/MA to connect TRIGA and TRIGB individually to a VXI TTL Trigger line. Both TRIGA and TRIGB can be individually enabled and set as input or output as described in **Figure 2-7**. An inversion bit is also provided to allow the user to configure the trigger for a rising or falling edge. All M/MAs on the carrier can be connected to the same VXI TTL Trigger line to synchronize the M/MAs.

Interrupts

The ANSI/VITA 12-1996 M-Module Specification specifies that an M/MA module may generate an interrupt. The VXI interrupt level is programmed by writing the desired level into the Interrupt Level field of the Interrupt Control Register (0x08 or 0x20). Writing a zero to the Interrupt Level field disables the interrupt for that M/MA.

M/MA modules can support Type A, B, or C interrupts. A Type A interrupter requires software to access the module to release the interrupt request, sometimes referred to as release on register access (RORA). A Type B interrupter releases the interrupt request during the hardware interrupt acknowledge cycle sometimes referred to as release on acknowledge (ROAK). A Type C interrupter is the same as a Type B interrupter, except the M/MA module also supplies an interrupt vector during the interrupt acknowledge cycle.

Type A and B interrupters must use the software programmable Interrupt Vector field of the Interrupt Control Register (0x08) for the upper byte of the VXI interrupt vector (VXI Status/ID) during the interrupt acknowledge cycle. To enable this action, set the IVE bit to 0 in the Interrupt Control Register. The lower byte of the interrupt vector is the logical address of the M/MA module. Type C interrupters provide their own upper byte of the interrupt vector during the interrupt acknowledge cycle.

The VXI specification recommends that VXI modules use the ROAK interrupt protocol. This recommendation can be supported by using an M/MA module the uses Type B or Type C interrupts or by simply setting the interrupt type (IT) bit to a 1 in the Interrupt Control register. Setting the IT bit to 1 causes the VX405C to release the VXI interrupt request during the hardware acknowledge cycle, regardless of the interrupt type used by M/MA module. For Type A interrupters, the VX405C will release the interrupt request to the VXI during the interrupt acknowledge cycle, but the interrupt from the M/MA will still be pending until the appropriate IO register is accessed. The VX405C will not issue another interrupt to the VXI from that M/MA until the M/MA's interrupt is cleared.

M/MA Module Identification

The ANSI/VITA 12-1996 M-Module Specification allows for an optional identification function called IDENT. This IDENT function provides information about the M/MA module and is stored in sixteen word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in I/O space and the data is read one bit at a time. Access to the IDENT is only guaranteed after a reset is performed.

The VX405C also supports the optional VXI-IDENT function introduced by Hewlett-Packard. This optional function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type registers. Details are shown in **Table 2-2.**

Table 2-2. The VX405C automatically checks the M/MA-Module for support of this optional function during power-up. If the VX405C detects support, then the VXI Manufacturer ID in the VXI ID register and the Required Memory and Model Code in the VXI Device Type register are changed to reflect the settings provided by the M/MA-Module.

Table 2-2 M/MA Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	(Module Dependent)
2	Revision Number	(Module Dependent)
3	Module Characteristics	(Module Dependent)
4-7	Reserved	
8-15	M-Module Specific	(Module Dependent)
16	VXI Sync Code	ACBA
17	VXI ID	VXI Manufacturer ID
18	VXI Device Type	Req'd Mem/Model Code
19-31	Reserved	
32-63	M-Module Specific	(Module Dependent)

Note: The VXI Device Type word contains two fields, bits 0-11 are the Model Code and bits 12-15 are the Required Memory, where:
Req'd Mem ⇨ $2^{(23-m)}$, where m is the value of the four bits
Model Code ⇨ manufacturer specified model number

Built in Test and Diagnostics

During power-up initialization, a basic built-in test function is performed. If an initialization failure is detected, the SYSFAIL lamp will light indicating a failure. Sysfail Inhibit can be used to help isolate the cause of the failure. **The Sysfail Inhibit is a VXI slot inhibit; therefore setting the inhibit bit on any M/MA module will inhibit SYSFAIL on all M/MA modules.**

Trouble Analysis Guide

The following is a general guide of the most common problems that may be encountered with the VX405C, along with a suggestion of the possible causes.

SYMPTOMS	POSSIBLE CAUSES
Bus time out on A16 Access	1. Logical address incorrectly set. 2. Card incorrectly installed. 3. M/MA enable switch not enabled. 4. Logical address Modulo Select switch not set as expected.
Unable to access M/MA memory/IO space	1. Attempting to access an improper address. 2. VXI memory setting for that M/MA not set to 2 × M/MA's required memory. 3. AAA bit in the Status/Control register not set to allow A32/A24 addressing. 4. A24/A32 switch set improperly. 5. Offset register not set correctly.

Chapter 3
M213

General Description

The M213 provide GPS timing in a single-wide M-Module format adhering to the ANSI/VITA 12-1996 specification for M-Modules.

Purpose of Equipment

The M213 can be used in a wide variety of applications where a precision timing control is required.

Specifications of Equipment

Module Key Features

- ANSI Standard M-Module (single-wide)
- Motorola Oncore M12+ GPS Timing Receiver
- M-module interface allows complete communication with M12+
- Active monitoring of PPS output indicates when a valid 1PPS output signal is available
- PPS output control (always off, always on, on when certain conditions met)
- Antenna bias power is switch selectable for +3V or +5V operation.
- External power pass-through for integration with other M-modules

Oncore M12+ Specific Features

- 12-channel parallel receiver design tracks up to 12 satellites simultaneously
- Code plus carrier tracking (carrier-aided tracking)
- Position filtering
- Antenna current sense circuitry
- 3-dimensional positioning within 25 meters, SEP (with Selective Availability [SA] disabled)
- Extensive control and status
- Satellite tracking
- PPS output control

- Latitude and longitude
- Height
- Time
- Selectable 1 or 100PPS output
- Time-Receiver Autonomous Integrity Monitoring (TRAIM) algorithm for checking timing solution integrity
- Automatic site survey

Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V +12V or EXTPWR -12V	0 ___ 0	mA mA mA
Input Voltage	EXTPWR	40	V
Supply Current	EXTPWR Pass-Through	2.0	A

AC CHARACTERISTICS

Parameter		Conditions	Specification	Units
GPS Timing General Characteristics				
	-Receiver		12	channels
	-Tracking capability	simultaneous vehicles	12	satellites
	-Operating Frequency	L1	1575.42	MHz
GPS Timing Performance Characteristics				
	-Acquisition Time, Time to First Fix (TTFF)	Hot (almanac, position, time, ephemeris) Warm (almanac, position, time) Cold (no stored information) Internal Reacquisition after blockage	<25 <50 <200 <1	sec. sec. sec. sec.
	-Positioning accuracy	selective availability disabled	<25	meters SEP
	-Timing accuracy [1]	using clock granularity message 1s average 6s average without clock granularity message 1s average 6s average	 <2 <6 <10 <20	 ns ns ns ns
	-Antenna requirements	Active antenna module with external gain Required gain [2] Bias Power Current draw	 18-36 3 or 5 80	 dBm V ma max.
PPS Output Electrical Characteristics (Front panel and internal connector)				
	-Output Level	High (V_{OH}) into 50Ω load Low (V_{OL}) into 50Ω load	2.0 0.4	V min. V max.
	-Output Impedance		50 ±3	Ω
	-Output Source/Sink Current		±50	mA
	-Propagation delay	from M12+ output	3.5 min., 9.0 max.	ns
	-Skew	front panel output to internal connector output (common-edge variation)	300	ps max.
	-Rise/Fall Time	from 0.8V to 2.0V / 2.0V to 0.8V	1.5	ns max.
PPSACT Output Electrical Characteristics (Front panel)				
	-Output Level	High (V_{OH}) into high impedance load Low (V_{OL}) into high impedance load	_._ _._	V min. V max.
	-Output Impedance		3 – 7	Ω typ
	-Output Source/Sink Current		±__	mA
External Power Supply				
	-Input Voltage		+10 to +30	Vdc

Notes:
1. 1PPS or 100PPS with position-hold active
2. As measured at receiver the M12+ RF connector

Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (106.2 mm) wide.

Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for double-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D8
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	not supported
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	FFB_{16}
Model Number:	$00D4_{16}$ (212 dec.)
VXI Model Code:	$0FDE_{16}$ (M212)

Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, www.vita.com

User's Guide, Motorola M12+ GPS Positioning And Timing Receivers, Synergy Systems, LLC, P/N STRMM12+ Rev. A, 24 Nov 03, P.O. Box 262250, San Diego, CA 92196, www.synergy-gps.com

User's Guide, GPS Oncore Revision 5.0, Motorola GPS Products, 08/30/02, www.motorola.com

Functional Description

Overview

The M213 utilizes control logic to interface the M-Module bus to a Motorola Oncore M12+ Timing Receiver. The M12+ is controlled internally through a serial interface. See applicable documents in Chapter 3 section Applicable Documents for details on the M12+. A simplified block diagram is shown in **Figure 3-1**.

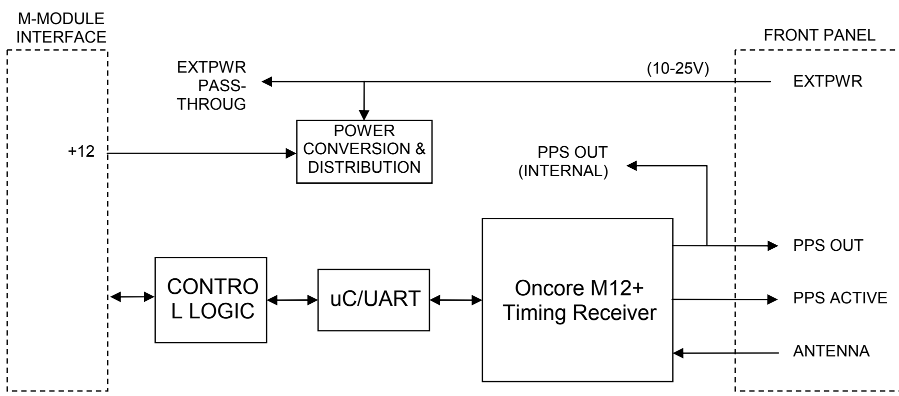


Figure 3-1 Functional Block Diagram

M-Module Interface

The M-Module Interface allows communication between the M213 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt and trigger capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for M modules.

Control Logic

The control logic provides the electrical interface between the M-module bus and the module. The control registers are contained within this logic. The control logic also monitors the PPS output and indicates when a valid 1PPS or 100PPS output signal is available (PPSACT). Status is directly is available through an M-module register and an interrupt can be generated on any change.

Microcontroller/

The microcontroller/UART provides the communication to and from the M12+ Timing module. An internal FIFO facilitates the software

UART communication.

Oncore M12+ Timing Receiver

The M12+ is GPS Timing Receiver module from Motorola. The M12+ internally provides extensive control and status of the GPS timing receiver, including antenna connection feedback, satellite tracking status, output quality indication, 1PPS output control, and a host of other position, almanac, and timing status and control functions. Detail information on this module can be found in the applicable documents shown in Chapter 3 Applicable Documents.

Power Conversion and Distribution

The main power for the module is obtained from either the M-module interface (+12V) or from an external supply through the front panel connector. Power is converted to appropriate levels and distributed to the individual components on the M213. The module uses the +12V supply from the M-module interface, unless an external supply is provided that is greater than +12V. To maintain GPS tracking, when the M-module interface is not powered, an external power supply must be provided.

To support integration with other M-modules, an external power pass-through connector is provided that simply passes the external supply voltage through, if it exists.

Physical Layout

The physical layout of the module is shown in **Figure 3-2**. A notch in the PCB is provided for the external power pass-through and the internal PPS output to allow cable access when the module is installed. A switch is provided to set the antenna bias voltage to either +3V or +5V.

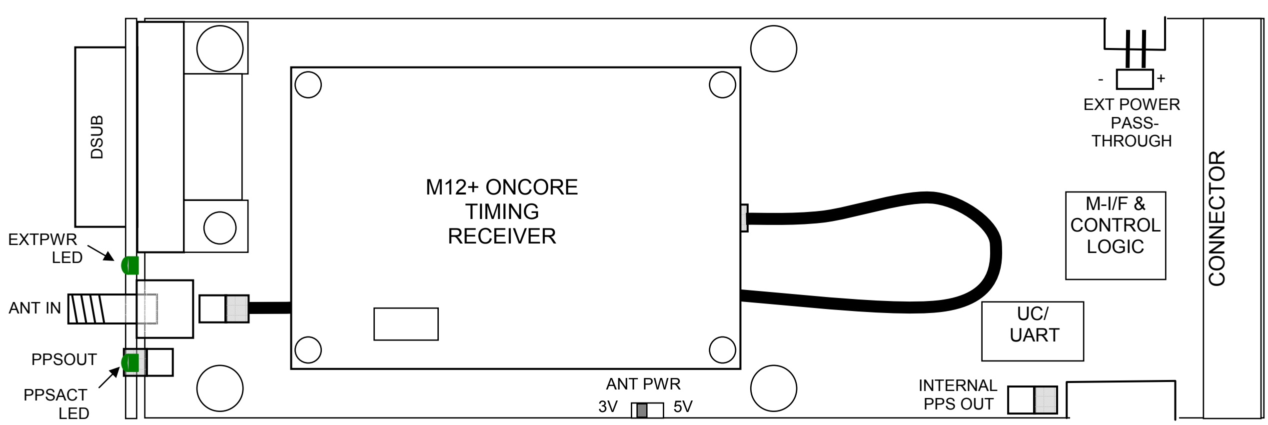


Figure 3-2 M213 Physical Layout

Input/Output Signals

The front panel input/output signals are as shown in **Figure 3-3** and are briefly described below. The connector shield of each of the connector is tied to chassis ground.

PPS

This MMCX connector provides the PPS output signal from the timing receiver. The signal is buffered through a 50Ω clock distribution driver. Under software control of the timing receiver, the output may be always ON, always OFF, or only ON if certain conditions are met. The LED indicates the ON/OFF status of the signal. The LED is visual indicator of the PPSACT signal (see below). *(5V CMOS logic levels, 50Ω output impedance)*

ANT

This SMA jack is for the antenna input. The bias voltage may be selected for 3V or 5V operation.

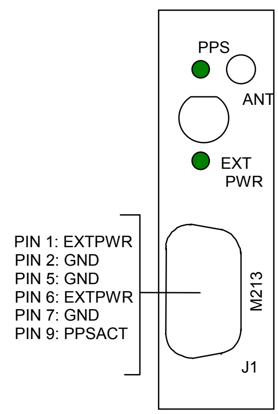


Figure 3-3 M213 Front Panel

EXTPWR

These two DSUB pins provide power to the M213 and to the external power pass-through connector. Module power can be provided through these front connectors or through the M-module +12V interface. The EXTPWR LED illuminates when external power above 8 to 10 volts is applied to the DSUB connector pins. *(+10 to +30Vdc)*

PPSACT

This DSUB pin indicates the status of the PPS output signal. The signal is high when the PPS signal is active. The PPS output from the GPS timing receiver is continuously monitored by the control logic. If the PPS output does not pulse within 1.3 seconds, the PPSACT signal will indicate inactive. *(active high, TTL output, low output impedance)*

GND

These DSUB pins are the return paths for the EXTPWR and the PPSACT signals. The pins are connected to the logic ground on the module.

Identification and Configuration Registers

I/O Registers

There are a variety of registers used to configure and control the M213 module. These registers are located in the IOSpace. The address map of the registers is shown in **Table 3-1**. Details of the registers are provided in **Figure 3-4**.

Table 3-1 I/O Address Map/Command Summary

M213 IO REG. (HEX)	REGISTER DESCRIPTION
00	Control/Status
02	Interrupt Control
04	UART Data Registers

Control/Status

M213 Reg.00 Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								-	-	-	-	-	-	-	-
Read	Not Used								-	-	-	-	-	-	PPS	-

PPS⇨PPS Active (0 = PPS output is not active, 1 = PPS output is active)

Interrupt Control

M213 Reg. 02 Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								IT	-	-	-	MIEN	-	PIEN	UIEN
Read	Not Used								IT	-	PPSI	URTI	MIEN	-	PIEN	UIEN

IT⇨ Interrupt Type (0 = Type A, software-end-of-interrupt (default), 1 = Type C, hardware-end-of-interrupt)
PPSI ⇨ PPS Interrupt Pending (1 = a PPS interrupt is pending (write a 1 to this bit to clear))
URTI ⇨ UART Interrupt Pending (1 = a UART interrupt is pending (write a 1 to this bit to clear))
MIEN ⇨ Master Interrupt Enable (0 = disabled (default), 1 = enable)
PIEN ⇨ PPS Interrupt Enable (0 = disabled (default), 1 = enabled)
UIEN ⇨ UART Interrupt Enable (0 = disabled (default), 1 = enabled)

Note: When using Type C interrupts (IT = 1), the interrupt pending bits 7-0 are presented as the interrupt vector during the interrupt acknowledge cycle. The MIEN bit is also cleared and must be re-enabled during the interrupt service routine. A PPSI interrupt occurs on any change, if enabled. A URTI interrupt only occurs when it becomes active.

UART Data Register

M213 Reg. 04 Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								Data							
Read	Not Used								Data							

Note: A write to Data transmits the byte to the M12+ timing receiver module. A read of Data receives one byte of data from the M12+ receive FIFO. A “Special Character, 0xFF” indicates that the FIFO is empty.

Figure 3-4 M213 I/O Registers

M-Module Identification PROM

The M213 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. **Figure 3-5** provides an example of how to read from the serial EEPROM.

The modules also support the VXI-IDENT function introduced by Hewlett-Packard. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in **Table 3-2**.

Table 3-2 M-Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00D5 (213 dec.)
2	Revision Number[1]	0001
3	Module Characteristics[2]	1068
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (RACAL INSTRUMENTS)
18	VXI Device Type[3]	0FDD (M213)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = module needs ±12V
11	0 = module does not need +5V
10	0 = trigger outputs not supported
9	0 = trigger inputs not supported
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address bus
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	FDD_{16} = RACAL INSTRUMENTS specified VXI model code for M213

Operation

The M213 is a register-based instrument that is controlled through a series of I/O registers. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system.

Rubidium Oscillator Communication

The UART Data Register is used to communicate with the M12+ Timing Receiver module. Data written to the register is serially transmitted to the M12+. Serial data received from the M12+ is converted into 8-bit data bytes and stored in a FIFO to be read by the user. The FIFO can store approximately 512 bytes. See Chapter 5 , "I/O COMMANDS" in the Motorola M12+ GPS Positioning And Timing Receivers User's Guide" for command details.

Interrupts

The M213 supports Type A and Type C interrupts as specified in the M-module specification. A Type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e., RORA)). A Type C interrupt releases the interrupt request during the interrupt acknowledge cycle (hardware-end-of-interrupt with vector (i.e., ROAK)) Type C interrupts provide an interrupt vector during an interrupt acknowledge cycle. Use the IT bit in the Interrupt Control Register to configure the desired type of interrupt.

> NOTE: For any interrupt to occur, the MIEN bit in the Interrupt Control Register must be set to a one.

For an interrupt to occur, the desired interrupt source must be enabled (PIEN or UIEN) and the master interrupt enable (MIEN) must be enabled in the Interrupt Control Register. For Type C interrupts, the interrupt vector is equal to the lower byte of the interrupt control register.

> NOTE: When using Type C interrupts, the MIEN bit is cleared during the interrupt acknowledge cycle. It must be re-enabled to receive another interrupt.

ID Prom

Refer to Chapter 4 section M-Module Identification PROM for a description of the ID PROM's function and contents. The ID PROM is a serial device and accessing it involves writing and reading a register in a sequential manner to acquire data. **Figure 3-5** provides a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*--------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
addr = 0xFE;                                          /* M/MA address for IDPROM */
id_addr = 0x80 | id_addr;                   /* 80 is the read opcode for the PROM */
write_eebyte (addr, id_addr);
read_eebyte (addr,&rdval);                  /* returns first byte of IDPROM */
tmpval = rdval << 8;                        /* upper byte of sync code word */
read_eebyte (addr,&rdval);                  /* returns first byte of IDPROM */
tmpval = tmpval | rdval;                    /* combine bytes of sync code   */
*value = tmpval;
write_word(addr, 0x0000);                   /* lower cs */
return;
}
/*--------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
write_word(addr, 0x0000);                   /* insure cs is initially low */
write_word(addr, 0x0004);                   /* initialize */
write_eebit(addr, 0x0001);                  /* start bit */
temp = value;
for (i=0;i<=7;i++){
write_eebit(addr, ((temp & 0x80)>>7));
temp = (temp << 1);
}
return;
}
/*----------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
temp = (0x0004 | (value & 0x0001));         /*  set data bit before clock */
write_word(addr, temp);
Delay(.000005);
temp = (0x0006 | (value & 0x0001));         /*  set data bit & clock */
write_word(addr, temp);
Delay(.000005);
return;
}
/*--------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
for (i=7;i>=0;i=i-1){
read_eebit (addr, &rdval);
temp = temp | ((rdval&0x01) << i);
}
*value = temp;
return;
}
/*-----------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value){
write_word(addr, 0x4);           /* lower clock bit */
Delay(.000005);
write_word(addr, 0x6);           /* raise clock bit */
Delay(.000005);
read_word (addr, value);
return;
}
/*-----------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 3-5 ID PROM Access Routine

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Chapter 4
M212

General Description

The M212 provides a precision Rubidium oscillator in a double wide M-Module format adhering to the ANSI/VITA 12-1996 specification for M-Modules (see exception below). A 1 pps output is an integral part of the design. An optional 1 pps input allows the unit to track a GPS or other external reference and display the difference between the input and the 1 pps generated by the Rubidium module (X72). The M212 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the M212 to be used in VXI, VME, PCI, cPCI, PXI and many other system architectures.

Note: Due to the physical height of the Rubidium oscillator the height on the back side of the module exceeds the allowable height specified in the M-Module specification. The height above the back of the PCB is approximately 0.25 inches. The user must ensure that this height will not interfere with other installed modules or shield assemblies for the specific carrier that is being used.

Purpose of Equipment

The M212 can be used in a wide variety of applications where a precision oscillator source is required.

Specifications of Equipment

Key Features

- 10MHz frequency
- Initial accuracy 5×10^{-11} @ 25°C
- Frequency Drift Stability 5×10^{-11} per month without optional 1PPS disciplining
- 1PPS input for long term stability (with optional 1pps disciplining)
- 1PPS output
- ANSI Standard M-Module (Double-wide)
- Full control of the Rubidium oscillator available

- Query serial number, operating hours, operating temperature, and event history
- Perform Self-test
- Front panel service and lock signals
- Operates from +10 to +25V power source from the front panel or internal connector
- Front panel lock indicator (indicates Rubidium lock or 1PPS input lock)
- Sine wave and square wave output

Specifications

MAXIMUM RATINGS

Parameter	**Condition**	**Rating**	**Units**
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V	100	mA
	+12V	0	mA
	-12V	0	mA
	EXTPWR (+10 to +25)	17	W

AC CHARACTERISTICS

Parameter	Conditions	Specification	Units
Dynamic Performance			
Sine wave Output			
- Frequency		10	MHz
- Power	Into 50Ω	7.8 ±10%	dBm
- Phase Noise	1Hz offset 10Hz offset 100Hz offset 1KHz offset 10KHz offset	−72 −90 −128 −140 −148	dBc/Hz max.
- Spurious	Harmonic Non-harmonic	−60 −60	dBc max. dBc max.
-Stability (Allan variance)	t = 1 second t = 10 seconds t = 100 seconds	3×10^{-11} 1×10^{-11} 3×10^{-12}	sec. max. sec. max. sec. max.
- Initial Accuracy	25°C	$\pm 5 \times 10^{-11}$	Hz
- Frequency Drift	25°C	$\pm 5 \times 10^{-11}$	per month
- Frequency Retrace	on-off-on: 24 hr, 48 hr, 12 hr @ 25°C	$\pm 2 \times 10^{-11}$	Hz
- Control	Range Granularity	$\pm 1 \times 10^{-6}$ $\pm 1 \times 10^{-12}$	Hz Hz
- Warm-up Time	Time to lock ($<5 \times 10^{-8}$) Time to $<1 \times 10^{-9}$	4 7.5	minutes minutes
Square wave Output			
- Level	ACMOS	5	V typ.
- Jitter	RMS	10	ps max.
MTBF	Ground benign	600,000	hrs

Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for double-wide M-Module modules. The nominal dimensions are 5.687” (144.5 mm) long × 4.183” (106.2 mm) wide.

Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for double-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D8
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	not supported
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	FFB_{16}
Model Number:	$00D4_{16}$ (212 dec.)
VXI Model Code:	$0FDE_{16}$ (M212)

Applicable Documents

ANSI/VITA 12-1996 - Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

X72 Precision Rubidium Oscillator Designer’s Reference, Symmetricom (formerly Datum), Document Number C/O/106031H

Installation

Unpacking and Inspection

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to RACAL Instruments. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to RACAL Instruments.

Handling Precautions

The M212 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

Installation of M/MA Modules

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in **Figure 4-1**. Secure the module through the holes in the bottom shield using the original screws.

> **CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.**

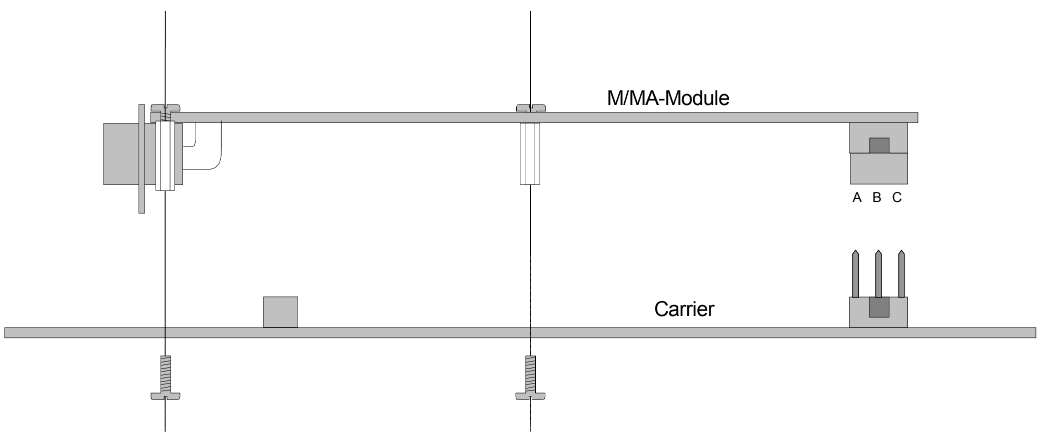


Figure 4-1 M-MODULE Installation

Preparation for Reshipment

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a RACAL Instruments system, then the original module shipping container and packing material may be re-used if it is still in good condition.

Functional Description

Overview

The M212 utilizes control logic to interface the M-Module bus to the Rubidium oscillator. The Rubidium oscillator is controlled internally through a serial interface. A simplified block diagram is shown in **Figure 4-2**.

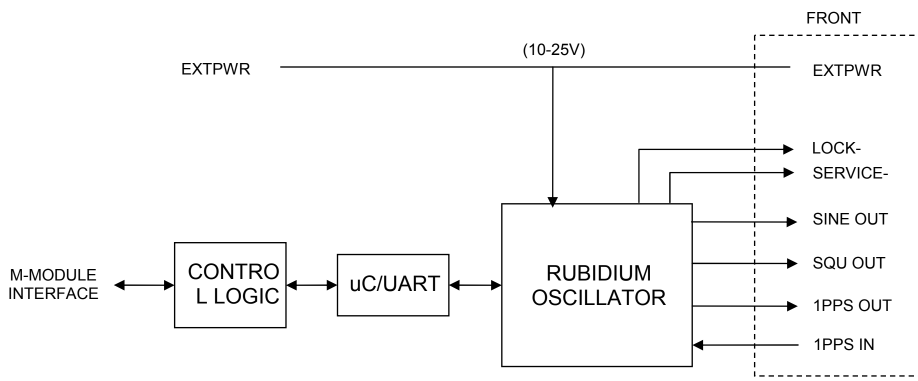


Figure 4-2 M212 Functional Block Diagram

M-Module Interface

The M-Module Interface allows communication between the M212 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt and trigger capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules.

Control Logic

The control logic provides the electrical interface between the M-module bus and the module. The control registers are contained within this logic.

Microcontroller/ UART

The microcontroller/UART provides the communication to and from the Rubidium oscillator. An internal FIFO facilitates the software communication.

Rubidium Oscillator

The Rubidium oscillator is a X72 Precision Rubidium Oscillator from Symmetricom (formerly Datum). See the designer's reference guide (C/O/106031H or latest) for more information.

Physical Layout

The physical layout of the module is shown in **Figure 4-3**. A notch in the PCB is provided for the EXTPWR connector to allow cable access when the module is installed. The CPLD and MICRO connectors are for factory use only. There are no configuration switches on the M212. Reference **Figure 4-4** for Connector configuration.

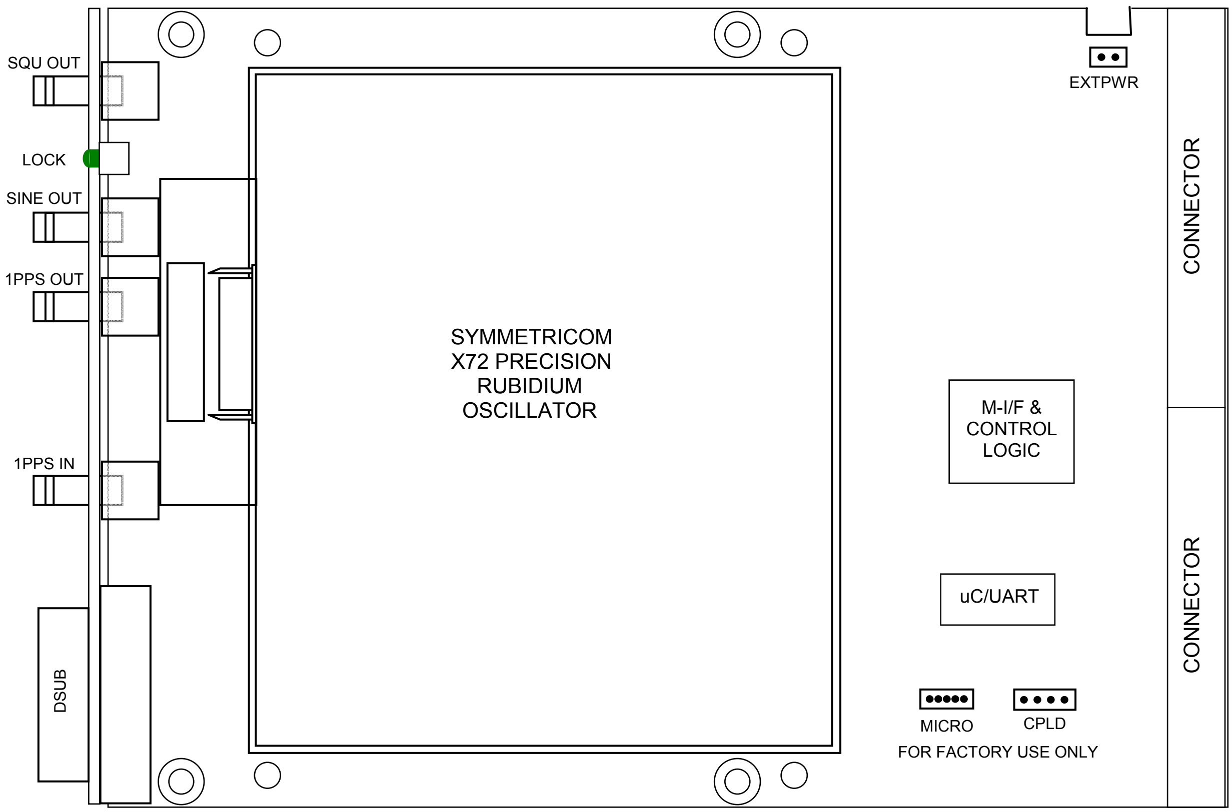


Figure 4-3 M212 Physical Layout

Pi n	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure 4-4 M/MA Interface Connector Configuration

Input/Output Signals

The front panel input/output signals are as shown in **Figure 4-5** and are briefly described below. The connector shield of each of the connector is tied to chassis ground.

EXTPWR

These two DSUB pins provide power to the Rubidium oscillator. Power can either be provided through these front connectors or through the EXTPWR connector located on the PCB. Power can be supplied to the Rubidium oscillator even when the M-module is not powered. *(+10 to +25Vdc)*

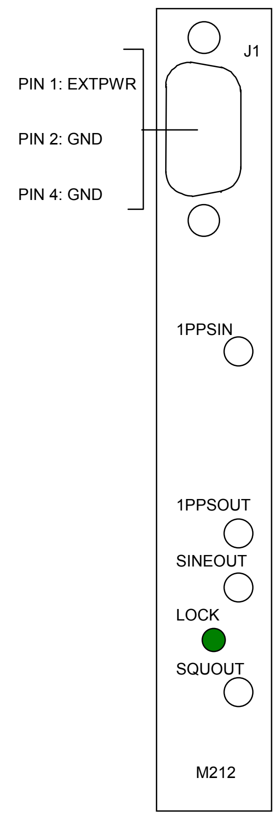


Figure 4-5 M212 Front Panel

LOCK

This DSUB pin indicates the lock status of the Rubidium oscillator. An LED also provided a direct visual indication of the lock status. When illuminated it indicates that the LOCK signal is active. *(active low, TTL output)*

SERVICE

This DSUB pin, when active, indicates that service on the Rubidium oscillator is required. *(active low, TTL output)*

1 PPSIN

This MMCX connector is the 1PPS input signal to the Rubidium oscillator. *(positive edge triggered, 3.3V ACMOS logic and 5V TTL logic compatible)*

1PPSOUT

This MMCX connector is the 1PPS output signal from the Rubidium oscillator. The output may be enabled/disabled through the Rubidium communication interface. *(3.3 ACMOS logic level)*

SINEOUT

This MMCX connector is the 10MHz sine wave output from the Rubidium oscillator.

SQUOUT

This MMCX connector is the 10MHz square wave output from the Rubidium oscillator. *(3.3 ACMOS logic level)*

Identification and Configuration Registers

I/O Registers

There are a variety of registers used to configure and control the M212 module. These registers are located in the IOSpace. The address map of the registers is shown in **Table 4-1**. Details of the registers are provided in **Figure 4-6**.

Table 4-1 I/O Address Map/Command Summary

M212 IO REG. (HEX)	REGISTER DESCRIPTION
00	Control/Status
02	Interrupt Control
04	UART Data Registers

Control/Status

M212 Reg. 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								-	-	-	-	-	-	-	-
Read	Not Used								-	-	-	-	-	SRV	LOK	-

SRV ⇨ Service (0 = normal operation, 1 = indicates that the Rubidium unit is nearing limits of frequency control and that service is required within several months)

LOK ⇨ Locked (0 = not locked, 1 = indicates that the output frequency is locked to the atomic resonance of rubidium)

Note: The SRV bit is only valid when LOK = 1.

Interrupt Control

M212 Reg. 02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								IT	-	-	-	MIEN	SIEN	LIEN	UIEN
Read	Not Used								IT	SRVI	LOKI	URTI	MIEN	SIEN	LIEN	UIEN

IT ⇨ Interrupt Type (0 = Type A, software-end-of-interrupt (default), 1 = Type C, hardware-end-of-interrupt)

SRVI ⇨ Service Interrupt Pending (1 = a Service interrupt is pending (write a 1 to this bit to clear))

LOKI ⇨ Lock Interrupt Pending (1 = a Lock interrupt is pending (write a 1 to this bit to clear))

URTI ⇨ UART Interrupt Pending (1 = a UART interrupt is pending (write a 1 to this bit to clear))

MIEN ⇨ Master Interrupt Enable (0 = disabled (default), 1 = enable)

SIEN ⇨ Service Interrupt Enable (0 = disabled (default), 1 = enabled)

LIEN ⇨ Lock Interrupt Enable (0 = disabled (default), 1 = enabled)

UIEN ⇨ UART Interrupt Enable (0 = disabled (default), 1 = enabled)

Note: When using Type C interrupts (IT = 1), the interrupt pending bits 7-0 are presented as the interrupt vector during the interrupt acknowledge cycle. The MIEN bit is also cleared and must be re-enabled during the interrupt service routine. SRVI and LOKI interrupts occur on any change, if enabled. URTI interrupts only occur when it becomes active.

UART Data Register

M212 Reg. 04

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								Data							
Read	Not Used								Data							

Note: A write to Data transmits the byte to the X72 oscillator. A read of Data receives one byte of data from the X72 receive FIFO. A “Special Character, 0xFF” indicates that the FIFO is empty.

Figure 4-6 M212 I/O Registers

M-Module Identification PROM

The M212 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time.

The modules also support the VXI-IDENT function introduced by Hewlett-Packard. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in **Table 4-2**.

Table 4-2 M/MA Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00D4 (212 dec.)
2	Revision Number[1]	0001
3	Module Characteristics[2]	0868
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	FFB (RACAL)
18	VXI Device Type[3]	0FDE (M212)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	1 = trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	FDE_{16} = RACAL INSTRUMENTS specified VXI model code for M212

Operation

The M212 is a register-based instrument that is controlled through a series of I/O registers. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access. A high–level driver may also be available for control.

Programming

Writing Registers

Normal 16-bit wide register values can be written in one write operation using 16-bit register access. However, some pulse parameters, such as the pulse period, pulse width, and pulse delay, require more than 16-bits. Special attention must be given when programming these values. To prevent a pulse parameter from changing until the entire value is written, the order of the write operations is important. The internal logic is configured to only accept the change when the high-order bits are written. Therefore, the application software must write the low bits first, then the middle bits, and lastly the high bits.

Rubidium Oscillator Communication

The UART Data Register is used to communicate with the Rubidium oscillator. Data written to the register is serially transmitted to the X72 oscillator. Serial data received from the X72 is converted into 8-bit data bytes and stored in a FIFO to be read by the user. The FIFO can store approximately 512 bytes. Use the Datum Serial Interface Protocol in the X72 Designer's Reference for command details.

Data Format

Run Mode Data Format (Customer Mode)

X72 outputs are all decimal DATA as "ASCII Coded Hex" except for echoed characters. The following example shows how data are encoded. Do not convert data to decimal when transmitting to the X72. All data are sent to the X72 and received back as "ASCII Coded Hex". The following example shows how data are encoded.

> NOTE: Flow control is not permitted in "Run Mode". Data sent to the X72 in run mode should not be encoded.

Data sent to the X72 in run mode should not be encoded.

Example of output from unit.
Example 1 (actual unit output)
Example of output from X72 after power applied to the unit.

```
X72 by Symmetricom, Inc., Copyright 2001
     SDCP Version 3.75 of 3/2001; Loader Version 2
     Mode CNN1  Flag 0004 [822F]ok

Unit serial code is 0009AB001B-h, current tuning state is 6
Crystal: 60000000hz, ACMOS: 10000000.0hz, Sine: 10000000.0hz
Ctl Reg: 029C, Res temp off: -1.5410, Lamp Temp off: -2.1142 FC:Enabled
Srvc: high

Enter Run Mode
FC Mode is enabled
f>
```

The following print out is an example of the response one gets by entering the letter “i” to get serial number and other facts of “*information*” on the X72:

```
r>i

X 7 2  by Symmetricom, Inc., Copyright 2004
     SDCP Version 5.02 of 4/2004; Loader Version 2
     Mode CN1B  Flag 0005

Unit serial code is 0009AB0018-h current tuning state is 6
 Crystal: 3938700hz, ACMOS: 989680.00000000hz, Sine: 989680.00000000hz
 Ctl Reg: 0204, Res temp off: BFC53F7D, lamp temp. off: c003B7E9,
 FC: enabled, Srvc: low
```

The following print out is an example of entering the letter “h” to get the “*help menu*” from the X72:

```
r>h
a: Set FC Mode
g: Setting the Lock Pin Functionality
f: Adjust DDS Frequency (delta e-11)
i: Info (show program info)
j: Display 1pps Delta Reg
k: Set 1pps TIC
l: Set Service Pin Sense
o: Set ACMOS Output Frequency ‘N’
p: Display Control Reg
q: Set Control Reg
t: Dave Tuning Data
w: Display Health Data
x: Exit Run Mode
y: Setting the Damping Factor and Tau Coefficients
r>
```

The following print out shows the response to the command for "w" for X72 "*Health Data*" (wellness):

```
r>w
AData:
  SCont: 6012
  SerNum: 18C
  PwrHrs: 18A
  PwrTicks: 11A6848
  LHHrs: 17E
  LHTicks: 83DBD0
  RHHrs: 17E
  RHTicks: 83D2E3
  dMP17: 41883621
  dMP5: 40A158E9
  dHtrVolt: 41381AF5
  PLmp: 3FAA43C6
  PRes: 3FA10F45
  dLVthermC: 39500000
  dRVthermC: B9DD8000
  dLVolt: 3F327288
  dMVoutC: 494005E0
  dTempLo: 00000000
  dTempHi: 42928000
  dVoltLo: 4134DC6A
  dVoltHi: 41C1CA16
  iFpgaCtl: 029E
  dCurTemp: 42690000
  dLVoutC: 3E25B538
  dRVoutC: 3E19A67E
  dmv2 demAvg: 3F337D72
```

The following print out shows how entering letter “a” followed by an integer sets the “*enable/disable*” feature of FC mode. Integer zero followed by <cr> disables FC mode and any nonzero integer followed by <cr> enables the FC mode.

```
r>a
<nonzero integer-><cr>
FC mode enabled
r>a
o<cr>
FC mode disabled
```

The following print out shows the “*control register*” contents by entering the letter “p”:

```
r>p
Control Reg: 029E
```

X72 1PPS Functions

The X72 can be configured to:

- Generate a rubidium controlled 1PPS signal.
- Measure the difference between an incoming 1PPS signal and the X72 1PPS
- Synchronize X72’s frequency and 1PPS output to the incoming 1PPS and provide very long holdover times.

When an externally generated 1PPS signal is applied to pin 19 of the J1 26 pin connector on a properly configured X72 the unit can provide the time interval error difference between the 1PPS input and the 1PPS generated inside of the X72. The difference is read via the RS232 communications “j” command. The “j” command displays the difference between the 1PPS input and the 1PPS generated internally by the X72. The “j” command produces a number representing the number of TICS in a delta register. If the X72 has a 60MHz crystal, each TIC is 16.7ns (1.67E-8). Note that this number is in hex format.

X72 1PPS Algorithm Operation

There are two parameters that can be modified by the user for 1PPS synchronization using the "y" command – Damping Factor and Tau.

- Damping factor – determines the relative response time and ringing in response to each step. Values should be between 0.25 and 4. Values less than 0.25 will default to 0.25 while values over 4 will default to 4.
- Tau (or time constant) – expressed in seconds and determines the time constant of the PLL for following a step in phase for the reference. The range of Tau is 5-100,000 seconds. Values outside this range will cause both the Damping Factor and Tau to change to the factory default settings.

Factory Default:

The factory default requires no inputs to the rubidium oscillator from the user. The default value for Damping Factor is 1 and the default Tau is 400. These values are a good starting point and will work well for most GPS applications.

Changing the "y" Coefficients

- At the "r>" prompt, press the y key, then the 1 key, then press Enter. (the 1 indicates that you wish to input the Damping Factor.).
- Input a value between 0.25 and 4 and then press Enter.
- At the "r>" prompt, press the y key, then press the 2 key, then press Enter. (the 2 indicates that you wish to input the Time Constant).
- Input a value between 5 and 100,000 and then press Enter.
- At the "r>" prompt, press the z key. This saves the 1PPS configuration data to non-volatile memory. If the y coefficients are not saved with the z command, the X72 will revert to the previously saved configuration upon restart. The X72 will respond with the following output.

```
r>z
Saving Tdata 2, serial number xx
1PPS Coefs saved
```

The "y" Coefficients – Factory Default

If the factory default values of Damping Factor = 1 and Tau = 400 are acceptable for your application, no modifications to the y coefficients are required. The X72 1PPS disciplining is enabled at the factory allowing the unit to work right out of the box. If the user wishes to return the y coefficients to the factory defaults, enter the value 0 for both the Damping Factor and Tau in the process described above. This will cause the X72 to operate at the factory default Damping Factor of 1 and Tau of 400.

The "j" Command

The j key can be pressed at any time to return the current value in hex format from the Delta Register as well as the 1PPS state (See the following **Table 4-3**). The output format will appear similar to the following:

```
r>j
Delta Reg: 39386F5 1ppsState:6
```

Table 4-3 1PPS States Returned with the j Command

Description	Expected Values	Action Being Performed
INITIALIZE0STATE	0	Start up initialization
INITIALIZE1STATE	1	Start up initialization
INITIALIZE2STATE	2	Start up initialization
HOLDOVERSTATE	3	Seeking useable 1PPS
JAMSYNC1STATE	4	Synch X72 output 1PPS to input
JAMSYNC2STATE	5	Synch X72 output 1PPS to input
DISCIPLINESTATE	6	Keep X72 output 1PPS aligned to input by controlling X72 frequency.
PIDCALCSTATE	7	Calculations for disciplining algorithm.
PDATEDDSSTATE	8	Update X72 DDS based on PIDCALSTATE output.
ALCSLOPESTATE	9	Calculate slope of incoming 1PPS vs. X72 1PPS during holdover.

The "g" Command

With the "g" command the user can change the X72 to operate in any of three modes which affect the output of the Lock Pin (pin 21). Note that this 1PPS mode can be changed by the user but cannot be saved. If power is cycled to the unit, it will revert to the factory default. The modes are:

0 = 1PPS Disciplining Disabled – Normal Rb Lock Pin functionality. Only the Rb loop needs to be locked to indicate a locked condition on pin 21.

1 = 1PPS Disciplining Enabled – Normal Lock Pin functionality. Only the Rb loop needs to be locked to indicate a locked condition on pin 21.

2 = 1PPS Disciplining Enabled – Requires both Rb loop to be locked AND 1PPS synchronization lock to indicate a locked condition on pin 21.

Notes:

1. **These numbers are in Hex format.**
2. **1ppsStates: 0-2 – Initialize; 3, 9 – Holdover; 6-8 – Disciplining**
3. **When connecting to a GPS receiver, the factory default mode is recommended. Start with y1 = 1 (DF) and Y2 = 400 TC in seconds). These values work well for most GPS receivers.**
4. **Use "z" command to save your settings.**
5. **X72 Rubidium system will lock approx. 5 minutes after startup.**
6. **X72 initial frequency must be less than +/- 3PPB for 1PPS to lock.**
7. **Initial 1PPS lock will occur between 3-5 minutes after both lock and valid 1PPS are present.**
8. **Confirm the firmware version by issuing the "i" command.**
9. ***xx* is a value returned which is the hex equivalent of the number of times the table has been written to . Tdata can be either 1 or 2.**

Calibration

The X72 is designed to stay within 5E-8 for 20 years without calibration. At the end of this period, the X72 should be returned to the factory for service.

Floating Point Number Representation

The host PC must convert Floating Point numbers output by the X72 to the host's own floating point using the definition shown in **Table 4-4**. Likewise, the host's floating point numbers must be converted to X72 coding before being sent to the X72.

Table 4-4 Floating Point Number Representation for DSIP

Floating Point Format – Single Precision

31 S	30 E7	29 E6	28 E5	27 E4	26 E3	25 E2	24 E1	23 E0	22 M22	21 M21	20 M20	19 M19	18 M18	17 M17	16 M16
15 M15	14 M14	13 M13	12 M12	11 M11	10 M10	9 M9	8 M8	7 M7	6 M6	5 M5	4 M4	3 M3	2 M2	1 M1	0 M0

Single precision floating point format is a 32-bit format, consisting of a 1-bit sign field, an 8 bit exponent field, and a 23-bit mantissa field. The fields are defined as follows:

Sign <S>: 0 = positive values; 1 = negative value

Exponent <E7-E0>: offset binary format

00 = special cases (i.e. zero)
01 = exponent value + 127 = -126
FE = exponent value + 127 = +127
FF = special cases (not implemented)

Mantissa <M22-M0>: fractional magnitude format with implied 1

1.M22M21…M1M0
Range: -1.9999998 e+127 to –1.0000000 e-126
+1.0000000 e-126 to + 1.9999998 e+127
(where e represents 2 to the power of)

Table 4-5 X72 Run Mode Commands

USER OUTPUT TO X72		RESPONSE TO HOST	NAME & DESCRIPTION OF COMMAND
Command	Data		
a	Set FC mode Example: a <zero or non zero intger> <cr>	*To be Specified*	Set Analog Frequency Control Mode This command toggles the analog input pin to the unit "Freq Cntl" between enable and disable. In Factory mode the default is enabled. During factory test the default is set to disable for shipping unless the customer ordered the default to be set enabled.
f	Desired frequency change from free running center frequency in parts to E-11 Example: for a +100E-11 change:"100<cr>" Example: for a -100E-11 change "-100<cr>"	*To be Specified*	Adjust Frequency Adjust Unit output frequency. Used to discipline the unit. The smallest incremental frequency change is 2E-12 (or "f.2"). Any value less than this will still be used. No illegal values. Unit always powers up at free running factory set frequency. This command is always relative to the free running frequency.
h	None	*To be Specified*	HELP command Displays menu.
i	None	*To be Specified*	Outputs Unit information. While dumping data, Clock outputs are not guaranteed to meet specifications during the use of this command.
o	N (example of command and data to give 10MHz for a VCXO of 60MHz is: "o3"	*To be Specified*	Loads the value of N to set the ACMOS output frequency. N is 1 to 65536. Output FACMOS is equal to crystal frequency divided by 2N. For values outside range, unit sends an illegal notice. E uses the previous valid setting.
p	None	*To be Specified*	Displays Control Register
q	Hex data to set or reset bits in the Control Register immediately follows the command (example "q3A")	*To be Specified*	Set Control Register Allows enabling or disabling of outputs.
w	None	*To be Specified*	Displays Health Monitor data

NOTE: To save changes to default settings for next power up:
Enter “t” command followed by “5987717” <cr> to save.
The output control status register (OSR) bit structure, control features and controlling factors are defined as shown below.

Table 4-6 X72 Output Control Status Register Structure

Bit #	Control	Description	Controller
0.*	Lamp Switch Power Boost -internal unit function	0 = Lamp Switch off 1 = Lamp Switch is on	Controlled by firmware – Automated Function
1.*	BIST Output	0 = Unit is locked 1 = Unit is not locked	Controlled by firmware – Automated Function
2.	FXO Enable	0 = Enable FXO output 1 = Disable FXO output	Default is set at Factory.
3.	1PPS Output Enable	0 = Enables 1PPS Output 1 = Disables 1PPS Output	Default is set to 1pps enabled at Factory Configuration.
4.	ACMOS Output Enable	0 = Enable Output 1 = Disables Output	Default is set to ACMOS enabled at Factory Configuration.
5.	C-field Boost	0 = Low C-field 1 = High C-field	Controlled by firmware – Automated Function
6.	SINE Output Enable	0 = Enables Output to 40% of max output 1 = Disables Output	Default is set to sine output enabled at Factory Configuration. SINE enable will not provide an output.
7.	SINE Output Level Adjust 1	0 = Zero Level 1 = Adds 30% of max Output	Controlled by firmware – set at factory
8.	SINE Output Level Adjust 2	0 = Zero Level 1 = Adds 20% of max Output	Controlled by firmware – set at factory
9.	SINE Output Level Adjust 3	0 = Zero Level 1 = Adds 10% of max Output	Controlled by firmware – set at factory
10.	SERVICE	0 = Unit is OK 1 = Unit requires Service	Controlled by firmware – Automated Function
11-15.	Reserved - Not Used		

*When altering the Control Register these bits are masked out by firmware, the Host will consider these bits as “DON”T CARE”.

Interrupts

The M212 supports Type A and Type C interrupts as specified in the M-module specification. A Type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e., RORA)). A Type C interrupt releases the interrupt request during the interrupt acknowledge cycle (hardware-end-of-interrupt with vector (i.e., ROAK)) Type C interrupts provide an interrupt vector during an interrupt acknowledge cycle. Use the IT bit in the Interrupt Control Register to configure the desired type of interrupt.

> NOTE: For any interrupt to occur, the MIEN bit in the Interrupt Control Register must be set to a one.

For an interrupt to occur, the desired interrupt source must be enabled (SIEN, LIEN or UIEN) and the master interrupt enable (MIEN) must be enabled in the Interrupt Control Register. For Type C interrupts, the interrupt vector is equal to the lower byte of the interrupt control register.

> NOTE: When using Type C interrupts, the MIEN bit is cleared during the interrupt acknowledge cycle. It must be re-enabled to receive another interrupt.

ID PPROM

The ID PROM is a serial device and accessing it involves writing and reading a register in a sequential manner to acquire data. **Figure 4-7** provides a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;                  /* 80 is the read opcode for the PROM */
  write_eebyte (addr, id_addr);
  read_eebyte (addr,&rdval);                 /* returns first byte of IDPROM */
  tmpval = rdval << 8;                       /* upper byte of sync code word */
  read_eebyte (addr,&rdval);                 /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;                   /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);                  /* lower cs */
  return;
}
/*-------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);                  /* insure cs is initially low */
  write_word(addr, 0x0004);                  /* initialize */
  write_eebit(addr, 0x0001);                 /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_eebit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*---------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));        /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));        /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*-------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_eebit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*----------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                     /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                     /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*----------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 4-7 ID PROM Access Routine

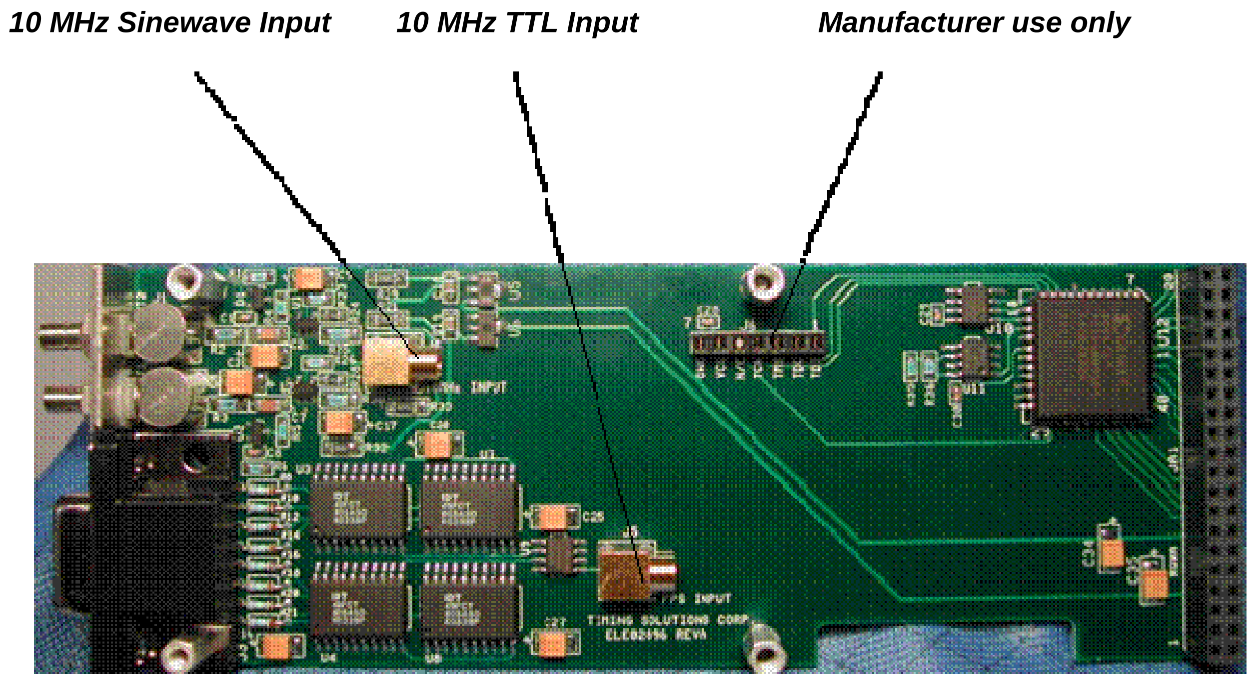
Chapter 5
M1708

General Description

The M1708 is a dual clock distribution amplifier housed in a standard single wide register based VXI M module. The module will accept one 10 MHz square wave signal and/or one 10 MHz sine wave input. The 10 MHz square wave signal is distributed to 8 outputs on a high density 15 pin D-Sub connector. The 10 MHz sine wave signal is distributed to two SMB connectors on the front panel. The module can be monitored through the register based interface. The M module interface is compliant with ANSI/VITA standard 12-1996.

Figure 5-1 M1708 Front panel

Figure 5-2 M1708 PWA component side



Interfacing to the M1708

Accessing the Module

EEPROM Identification

This module supports the M-Module serial EEPROM identification function at address 0x80:

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	06AC
2	Revision Number [1]	0000
3	Module Characteristics [2]	1800
4-7	Reserved	0000
8	M-Module Specific	5757
9	M-Module Specific	572E
10	M-Module Specific	5459
11	M-Module Specific	4D49
12	M-Module Specific	4E47
13	M-Module Specific	2E43
14	M-Module Specific	4F4D
15	M-Module Specific	2020
16	VXI Sync Code	ACBA
17	Racal VXI Code	0FFB
18	VXI Device Type [3]	F6AC
19-31	Reserved	0000
32-63	M-Module Specific	(not used)

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.

2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = module needs ±12V
11	1 = module needs +5V
10	0 = trigger outputs not supported
9	0 = trigger inputs not supported
8/7	00 = no DMA requestor
6/5	00 = no interrupter
4/3	00 = 8-bit data
2/1	00 = 8-bit address bus
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$6AC_{16}$ = RACAL INSTRUMENTS specified VXI model code for 1708

Address Decoding

Address A7 is the only decoded address bit.

Address:0x00 is reflected up to address 0x7f

Address:0x80 is reflected up to address 0xff

Address 0x00 reads the latched status of the 10MHz Square Wave TTL Outputs.

The latched outputs are cleared at the end of each read. To obtain the current state of the output, read the port to get any failures since the last read. Read again to get any current failures.

Bits7:0 correspond to TTL outputs 8:1 where a 1 in a bit position indicates a failure and a 0 indicates no failure.

Address 0x80 controls the serial EEPROM and contains the latched output status of the 10MHz sine wave. The output status is reported as fault if the output level is less than approximately 2 dBm.

The latched outputs are cleared at the end of each read. To obtain the current state of the output read the port to get any failures since the last read. Read again to get any current failures.

Bits7:3 - not used read 0

Bit2 - Out2 Status 1=fault, 0=good

Bit1 - Out1 Status 1=fault, 0=good

Bit0 - Serial EEPROM Data - ignore

Connectors

Refer to Appendix D for connector and pin assignments.

Specifications

Electrical Specifications

Item	Specification
Module Current	+5 V: 0.01 A +12 V: 0 A -12 V: 0 A +24 V: 0 A -24 V: 0 A -5.2 V: 0 A -2 V: 0 A
TTL Signal Inputs	Impedance: 50 Ω/ Nominal input 3 V peak, 5 V Maximum
Connectors	Input : 2 MMCX Female Output : 2 SMB Female, 1 high density DB15 Female Standard M module carrier board connector, A8/D16 Register-based M-Module Circuitry
Sine wave output parameters	Gain : 3.5 dB Level : Maximum 15dBm into 50 Ω Isolation between outputs : > 90 dB
TTL output parameters	Rise and Fall times < 3.0 ns Skew (channel to channel) : < 500 ps Jitter : < 50 ps rms High level : 3 V minimum into 50 Ω Isolation between outputs : > 80 dB
Spectral Purity (sine outputs)	Harmonics : < -40dBc Spurious : < -80 dBc
Phase Noise	10 Hz offset : -90 dBc/Hz 100 Hz offset : -128 dBc/Hz 1 kHz offset : -140 dBc/Hz 10 kHz offset : -147 dBc/Hz

Environment Specifications

Item	Temperature	Relative Humidity	Altitude
In Use	0°C to 50°C	0% to 90% (non-condensing)	3,000 meters (9,843 feet)
Storage	-40°C to 70°C	0% to 90% (non-condensing)	
Transportation	-40°C to 70°C	0% to 90% (non-condensing)	

Physical Specifications

Item	Specification
Width	Standard single width M module
Height	Standard single width M module
Depth	Standard single width M module
Weight	Approximately 0.2 kg

Chapter 6
M210

General Description

The M210 provides distribution of clock signals to other devices. The module accepts two analog input signals and provides TTL and ECL distribution. The input signals are passed through high speed comparators that convert the analog level to a digital signal. The digital signals are individually buffered to provide the TTL and ECL outputs.

The module is physically implemented on a double-wide M-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules.

Purpose of Equipment

The M210 can be used in a wide variety of applications including functional verification of digital systems, signal simulation, design verification, and research and development that require the distribution of clock and timing signals.

Specifications of Equipment

Key Features

- Two Input Channels
- 100MHz Maximum Frequency
- Each input channel supports 1 ECL output and 4 TTL outputs
- Input A or B can be configured to support 8 TTL outputs [1]
- Input High and Low levels are individually programmed for each input
- Trigger input with software programmable threshold
- Non-volatile potentiometers retain setting when power is off
- Switch settings allow full operation at factory set levels (no software programming required)
- M-Triggers supported (source for input channels or trigger output)

[1] Input A or B can drive either four TTL outputs or all eight TTL outputs. If Input A is configured to drive eight TTL outputs, then Input B drives no TTL outputs and vice versa. The ECL output of each input signal is not affected.

Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption (power is shared by both M-module connectors)	+5V +12V -12V	1200 50 400	mA mA mA
Input Voltage (INA, INB, TRIGIN)	no damage	±10	Vrms

AC CHARACTERISTICS

Parameter	Conditions	Min	Limit Typ.	Max	Units
Common Input Characteristics					
Voltage Range		-5.0		+5.0	V
Input Impedance	Switch = 50Ω Switch = Hi-Z	48 10K	50 10.3K	52 10.6K	Ω Ω
Level Adjust Resolution	8 bit		39		mV
Threshold Level Accuracy	Input Impedance = 50Ω Input Impedance = Hi-Z	±7% + 150mV ±10% + 150mV			% + mV % + mV
Frequency	Input Impedance = 50Ω Input Impedance = Hi-Z	0 0		100 50	MHz MHz
Width		3		∞	ns
INA/INB Input Characteristics					
High Threshold Level Range[1]	Software programmable	-5.0		+5.0	V
Low Threshold Level Range[1]	Software programmable	-5.0		+5.0	V
Fixed Factory Default Levels	High Level Low Level		+2.15 +1.85		V V
Trigger Input Characteristics					
Input Threshold	Software programmable	-5.0		+5.0	V
Fixed Factory Default Level			+2.0		V
TTL Output Characteristics					
Impedance[2]			12.5		Ω
Output Levels	Load = 50Ω, V_{OL} V_{OH}	 3.0		0.5	V V
Propagation Delay	INA or INB to TTLOUT MTRIG to TTLOUT		14 24	21 30	ns ns
ECL Output Characteristics					
Type	10K Series ECL				
Termination	499Ω pull downs (-5.2V) on both lines				
Propagation Delay	INA or INB to ECLOUT MTRIG to ECLOUT		5 14	7 21	ns ns
Trigger Output Characteristics					
Impedance			50		Ω
Output Levels	Load = 50Ω, V_{OL} V_{OH}	 2.5		0.4	V V
Width		3		∞	ns
Propagation Delay	TRIGIN to TRGOUT		14	21	ns
Skew	between TRGOUT1 and TRGOUT2			1.0	ns

Notes:
1. The high level must be higher than the low level for proper operation.

2. Four output drivers with 50Ω source impedance each are used in parallel

Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for double-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (52.9 mm) wide.

Bus compliance

The module complies with the ANSI/VITA 12-1996 Specification for double-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	not supported
DMA:	not supported
Triggers:	not supported
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00D2_{16}$ (210 dec.)

Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

Functional Description

Overview

The M210 uses high speed comparator and ECL logic to provide low propagation delay signal distribution of two input signals. Each input signal is buffered and distributed to TTL and ECL outputs. A TRGIN function provides limited distribution for a third input. The module can be configured to handle a variety of input signals. A simplified block diagram is shown in **Figure 6-1**.

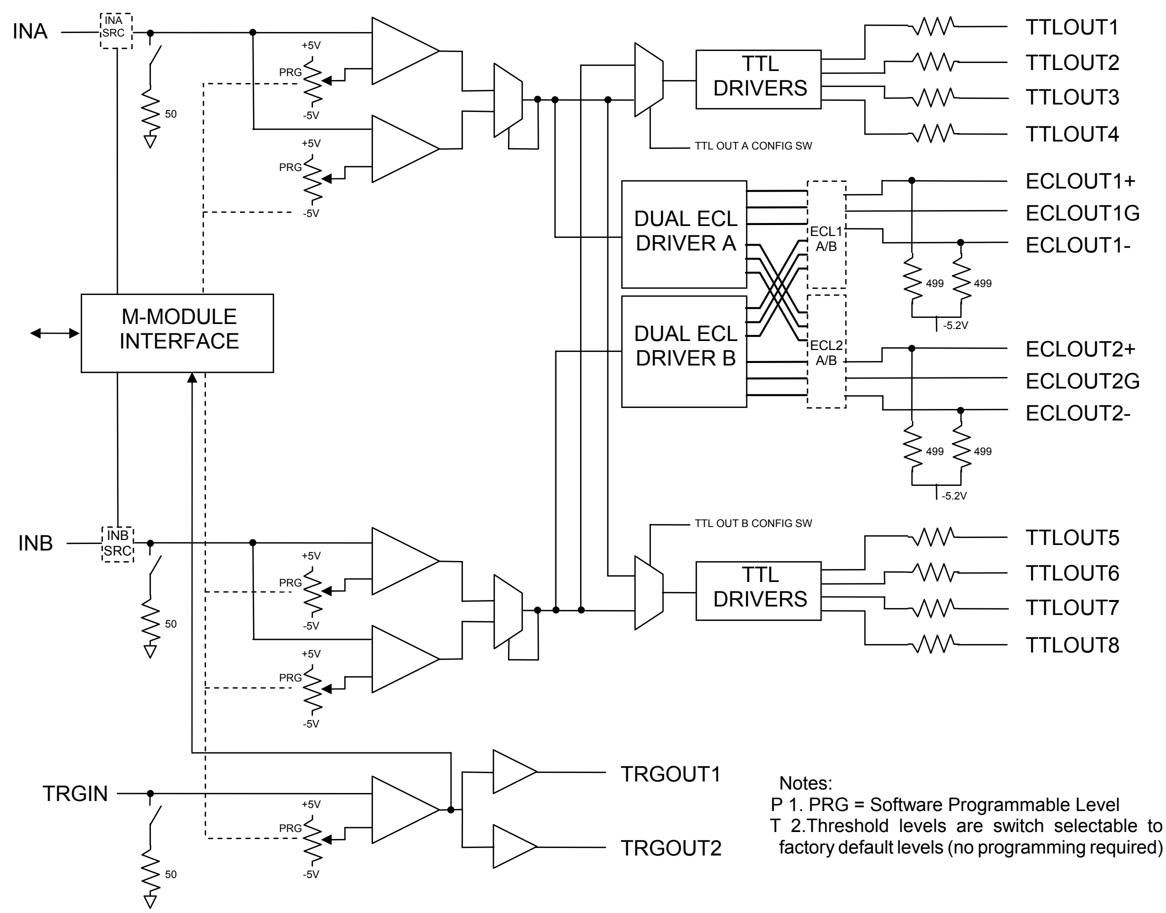


Figure 6-1 Functional Block Diagram

M-Module Interface

The M-Module Interface allows communication between the M210 and the carrier module. The interface is an asynchronous 16-bit data bus. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules. The interface also permits the mapping of M-module triggers as sources for the two standard inputs or as a destination for the TRGIN input signal.

Input Comparators

Input comparators provide high speed analog to digital conversion with programmable high and low levels. The comparators are configured to provide a hysteresis window for the input signal. As an input signal transitions from low to high, it must exceed the high threshold level to produce a high at the window comparator output. As an input signal transitions from high to low, it must fall below the low threshold level to produce a low at the window comparator output.

The comparator threshold levels can be either programmable or set to a factory default value. A hardware configuration switch provides this selection. The programmable threshold levels are set by programming a group of digitally programmable potentiometers. These potentiometers are non-volatile so they retain their setting even when power to the module is off.

The source of the input comparators is switch selectable as either the front panel input connectors or the internal M-module trigger lines. Input impedance is also switch selectable as either 50 Ohms or HI-Z.

TTL Drivers

Eight TTL outputs provide TTL compatible signal distribution of the input signals. Each input can be distributed to four TTL outputs or the module can be configured to distribute a single input to all eight TTL outputs.

Each TTL output consists of four output buffers in parallel. The output source impedance of each individual driver is 50Ω, thus providing an overall output source impedance of 12.5Ω that can drive TTL compatible logic levels into a 50Ω load.

ECL Drivers

Two ECL outputs provide ECL compatible signal distribution of the inputs. The source (INA or INB) of the ECL signals can be selected for each ECL output. The differential ECL outputs are terminated through 499Ω resistors to -5.2V.

Trigger Input Comparator and Distribution

The TRGIN function provides limited distribution for a third input. The TRGIN signal is distributed to two TRGOUT connectors (internal PCB mounted) and can programmatically be distributed to the M-Module trigger lines. The input comparator logic is similar to the standard inputs, however a hysteresis window in not provided. Instead, a single threshold level can be programmed or set to a factory default level as selected by a hardware configuration switch.

Hardware Configuration

The M210 contains a variety switches that select the various configurations of the module including: input impedance of the inputs, the output configuration of the inputs, the threshold levels of inputs, and the source of the inputs. The switches are only accessible with the module removed from the carrier and are located as shown in **Figure 6-2**.

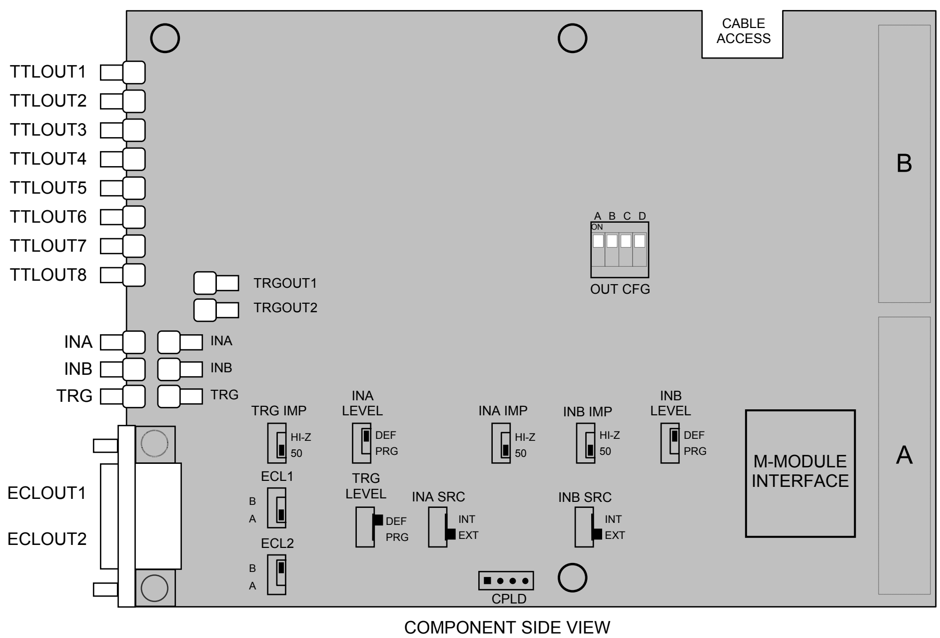


Figure 6-2 M210 Hardware Configuration Switches

INA IMP Switch	This switch selects the input impedance of the input A signal to be 50Ω or high impedance (~10KΩ).
INB IMP Switch	This switch selects the input impedance of the input B signal to be 50Ω or high impedance (~10KΩ).
TRG IMP Switch	This switch selects the input impedance of the trigger input signal to be 50Ω or high impedance (~10KΩ).
INA SRC Switch	This switch selects whether the INA signal come from the internal M-module trigger input or from the external front panel connector.
INB SRC Switch	This switch selects whether the INB signal come from the internal M-module trigger input or from the external front panel connector.
INA LEVEL Switch	This switch selects whether the input A threshold levels are software programmable or set to the fixed factory default levels of high = +2.15V, low = +1.85V (no programming required).
INB LEVEL Switch	This switch selects whether the input B threshold levels are software programmable or set to the fixed factory default levels of high = +2.15V, low = +1.85V (no programming required).
TRG LEVEL Switch	This switch selects whether the trigger input threshold level is software programmable or set to the fixed factory default level of +2.00V (no programming required).
ECL1 Switch	This switch selects whether the ECL1 signals are from INA or INB.
ECL2 Switch	This switch selects whether the ECL2 signals are from INA or INB.
OUT CFG Switch	These switches configure the source of the TTL outputs and select the operational mode of the logic.

TTL Output 1-4	IN CFG Switch A
Input A Drives Outputs (Normal)	OFF
Input B Drives Outputs	ON

TTL Output 5-8	IN CFG Switch B
Input B Drives Outputs (Normal)	OFF
Input A Drives Outputs	ON

Operational Mode	IN CFG Switch D
Normal	OFF
Special Mode	ON

Note: Switch C is not used.

INPUT/OUTPUT Signals

The front panel input/output signals are as shown in **Figure 5-1** and are briefly described below. MMCX jack receptacles are used for the TRG, INB, INA, and TTLOUT signals and a 9-pin DSUB plug provides connection to the ECLOUT1 and ECLOUT 2 signals. In addition to the front panel connectors, MMCX connectors are provided on the internal side of the PCB for the INA, INB, TRG, TRGOUT1, and TRGOUT2 signals. These connectors facilitate integration with other M-modules. Cable access is provided through a notch on one side the board (see **Figure 6-3**).

ECLOUT1 + and ECLOUT1+

These signal contacts are the ECL output positive signals.

ECLOUT2 - and ECLOUT2-

These signal contacts are the ECL output negative signals.

ECLOUT1G and ECLOUT2G

These signal contacts are the ECL output ground signals.

TRG

This MMCX connector is the TRGIN signal input. TRGIN can be input through this connector or through the internal PCB MMCX connector.

INB

This MMCX connector is the INB signal. INB can be input through this connector or through the internal PCB MMCX connector.

INA

This MMCX connector is the INA signal. INA can be input through this connector or through the internal PCB MMCX connector.

TTLOUT1-8

These MMCX connectors are the TTL output signals.

TRGOUT1 and TRGOUT2

These internal PCB mounted MMCX connectors are the distributed TRGOUT signals.

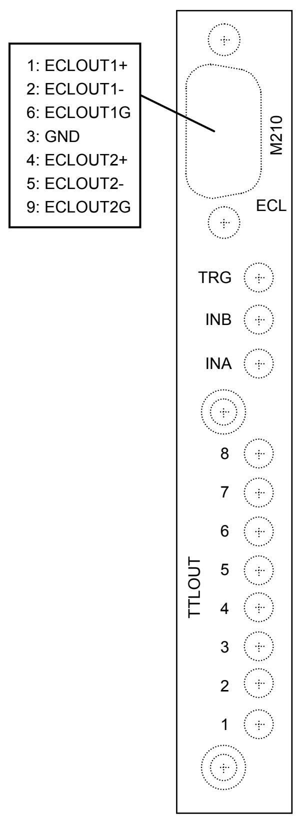


Figure 6-3 M210
Front Panel

Identification and Configuration Registers

I/O Registers

There are a variety of registers used to configure and control the M210 module. These registers are located in the IOSpace. The address map of the registers is shown in **Table 6-1**. Details of the registers are provided in **Figure 6-4**.

Table 6-1 I/O Address Map/Command Summary

IO REG. (HEX)	REGISTER DESCRIPTION
00	Configuration
02	Input A Threshold Level Control
04	Input B Threshold Level Control
06	Trigger Threshold Level Control

M210 Reg. 00

Configuration

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write											TRGO		SRCB		SRCA	
Read											TRGO		SRCB		SRCA	

SRCA ⇨ Input A Source
- 0 0 Front Panel
- 0 1 M-Trigger A
- 1 0 M-Trigger B
- 1 1 not used

SRCB ⇨ Input B Source
- 0 0 Front Panel
- 0 1 M-Trigger A
- 1 0 M-Trigger B
- 1 1 not used

TRGO ⇨ Input Trigger Output
- 0 0 none (internal SMA connectors only)
- 0 1 M-Trigger A
- 1 0 M-Trigger B
- 1 1 Both M-Trigger A & B

Note: The INA SRCA and/or INB SRC switches must be configured to INT to use the M-Triggers as inputs.

M210 Reg. 02

Input A Threshold Level Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													SELA	-	DIA	CLKA
Read													SELA	-	DIA	CLKA

SELA ⇨ Select Input A Threshold Level potentiometer (1 = active, 0 = inactive)
DIA ⇨ Data input signal to Input A Threshold Level potentiometer
CLKA ⇨ Clock signal to Input A Threshold Level potentiometer

Notes:
1. These bits directly control the 3-wire serial interface to the potentiometer. See Chapter 6 section Programming Threshold Levels for programming details. A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit.
2. The INA LEVEL switch must be set to PRG for the programmed threshold to take affect.

M210 Reg. 04

Input B Threshold Level Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													SELB	-	DIB	CLKB
Read													SELB	-	DIB	CLKB

SELB ⇨ Select Input B Threshold Level potentiometer (1 = active, 0 = inactive)
DIB ⇨ Data input signal to Input B Threshold Level potentiometer
CLKB ⇨ Clock signal to Input B Threshold Level potentiometer

Notes:
1. These bits directly control the 3-wire serial interface to the potentiometer. See Chapter 6 section Programming Threshold Levels for programming details. A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit.
2. The INB LEVEL switch must be set to PRG for the programmed threshold to take affect.

Figure 6-4 M210 I/O Registers

M210 Reg. 06

Trigger Threshold Level Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													SELT	-	DIT	CLKT
Read													SELT	-	DIT	CLKT

SELT ⇨ Select Trigger Threshold Level potentiometer (1 = active, 0 = inactive)
DIT ⇨ Data input signal to Trigger Threshold Level potentiometer
CLKT ⇨ Clock signal to Trigger Threshold Level potentiometer

Notes:
1. These bits directly control the 3-wire serial interface to the potentiometer. See Chapter 6 section Programming Threshold Levels for programming details. A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit.
2. The TRG LEVEL switch must be set to PRG for the programmed threshold to take affect.

Figure 6-4 M210 I/O Register (continued)

Module Identification

The M210 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial PROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in Chapter 6 section ID PROM. Data can not be written to the PROM.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the PROM to 64 words and includes VXI compatible ID and Device Type Registers. Details are shown in **Table 6-2**.

Table 6-2 M-Module PROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00D2 (210 dec.)
2	Revision Number[1]	0000
3	Module Characteristics[2]	1E68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (RACAL INSTRUMENTS)
18	VXI Device Type[3]	FFE1 (M210)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	1 = trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FE1_{16}$ = RACAL INSTRUMENTS specified VXI model code for M210

Operation

The M210 is a register-based instrument that is controlled through the I/O registers. The module can also be operated without any software control, if the default input levels are acceptable (see Chapter 6 section Hardware Configuration for switch details). The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

Programming Threshold Levels

The input threshold levels are programmed by writing bit values to the Input Threshold Level Control registers (Reg. 00 and 02). A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit. The CLKx and DIx bits directly control the serial bus signals connected to the digital potentiometer. The SELx bit must be set to 1 at least one write cycle before writing a 1 to the CLKx bit. The bits are written by sequentially writing to the control registers according to **Figure 6-5**.

Channel Input Programming:

→ Bits are written in this direction (Bit 0 is first bit written, Bit 16 is last bit written)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	MSB	Input X Low Threshold Level						LSB	MSB	Input X High Threshold Level						LSB

X ⇨ Don't Care

Trigger Input Programming:

→ Bits are written in this direction (Bit 0 is first bit written, Bit 16 is last bit written)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	X	X	X	X	X	X	X	MSB	Trigger Input Threshold Level						LSB

X ⇨ Don't Care

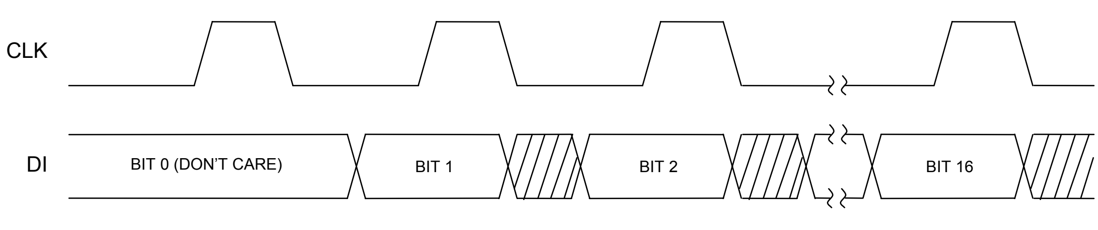


Figure 6-5 Potentiometer Serial Programming

ID PROM

Refer to Chapter 4 section M-Module Identification PROM for a description of the ID PROM's function and contents. Reading data from the ID PROM involves writing and reading a register in a sequential manner. Data can not be written to the PROM. **Figure 6-6** provides a general description of the code sequence necessary to read the information from the PROM. The PROM is compatible with a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*--------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;                /* 80 is the read opcode for the PROM */
  write_prbyte (addr, id_addr);
  read_prbyte (addr,&rdval);               /* returns first byte of IDPROM */
  tmpval = rdval << 8;                     /* upper byte of sync code word */
  read_prbyte (addr,&rdval);               /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;                 /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);                /* lower cs */
  return;
}
/*--------------------------------------------------------------------*/
int write_prbyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);                /* insure cs is initially low */
  write_word(addr, 0x0004);                /* initialize */
  write_prbit(addr, 0x0001);               /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_prbit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*----------------------------------------------------------------------*/
int write_prbit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));      /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));      /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*--------------------------------------------------------------------*/
int read_prbyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_prbit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-----------------------------------------------------------------------*/
int read_prbit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                   /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                   /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-----------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.

*2 **NOT** actual code and should be treated as a modeling tool only.*

Figure 6-6 ID PROM Access Routine

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Chapter 7
M1714

GENERAL DESCRIPTION

The M1714 provides 128 channels of digital I/O in a double-wide M-Module format adhering to the ANSI/VITA 12-1996 specification for M-Modules. This M-Module resides in a VX405C carrier for installation into a VXI chassis.

Specifications of Equipment

Use the original packing material when returning the 3352 to Racal Instruments for calibration or servicing. The original shipping container and associated packaging material will provide the necessary protection for safe reshipment.

If the original packing material is unavailable, contact Racal Instruments Customer Service for information.

Key Features

- Digital I/O - TTL Compatible
- 128 channels broken up into 16 groups of 8 bits each
- Directional Programming - each group of 8 bits can be programmed as either an input or output.
- Four 68-pin VHDCI front panel connectors.
- ‘Power’, ‘Activity’ and ‘BIST Fail’ front panel indicators.
- Built-in Self Test (BIST)

Specifications

Digital I/O 5V Bus

	Min	Max
V_{IH} (V)	2.0	5.5
V_{IL} (V)	-0.5	0.8
V_{OH} (V)	2.4	
V_{OL} (V)		0.45

Channel-To-Channel skew

20 ns, Max, across all 128 pins

Drivers -	74ACT244 with a 22 ohm series with 10K pull-up connected to +5V
Receivers -	74ACT373 with 820 ohm series resistor
Shock	15g, 11 ms, ½ sine wave
Vibration	0.33 mm. P-P, 5-55 Hz
Temperature	
	Operating 0°C to +55°C
	Non-operating -40°C to +75°C
Relative Humidity	85%, non-condensing at < 30°C
Altitude	
	Operating 10,000 feet
	Non-operating 15,000 feet
MTBF	765,387 hours (MIL-HDBK-217E)
Dimensions	double-wide M-Module (4.183" X 5.837")

Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for double-wide M-Module modules. The nominal dimensions are 5.837" X 4.183".

Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for M-Modules.

Module Type:	M-Module
Addressing:	A08
Data:	D8
Interrupts:	not supported
DMA:	not supported
Triggers:	not supported
Identification:	not supported
Model Number:	'9C'h
Revision Number:	'01'h

Applicable Documents

ANSI/VITA 12-1996Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, www.vita.com

Ordering Information

Listed below are part numbers for the M1714 Digital I/O M-Module.

ITEM	DESCRIPTION	PART #
M1714 M-Module	128 Channel Digital I/O	405262
Additional Manual		980900

FUNCTIONAL DESCRIPTION

Overview

The M1714 utilizes control logic to interface the M-Module bus to a series of digital I/O ports. The

I/O ports are driven and received via four 68-pin connectors mounted on the front panel. A simplified block diagram is shown in **Figure 7-1**.

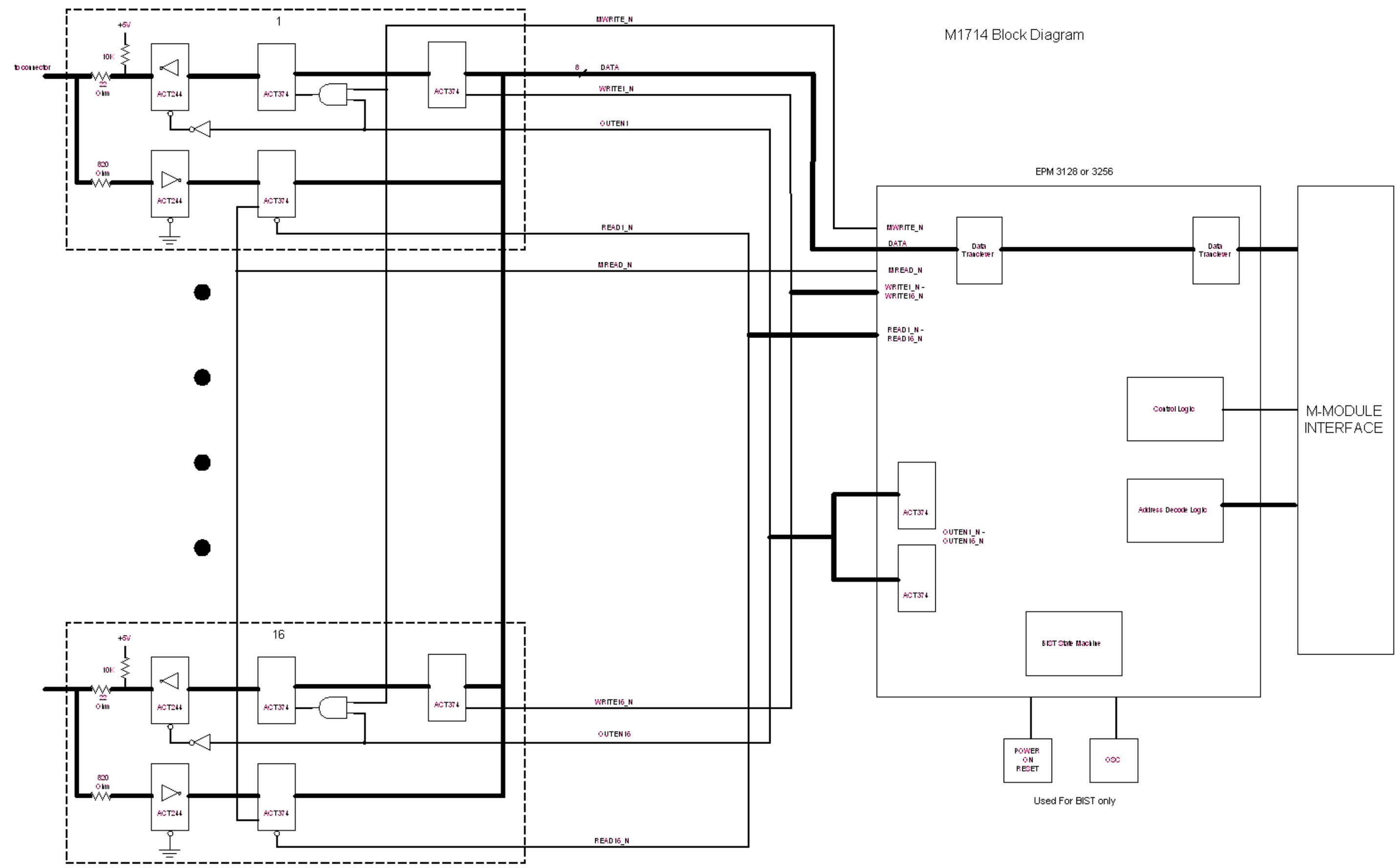

Figure 7-1 M1714 Block Diagram

M-Module Interface

The M-Module Interface allows communication between the M1714 and the carrier module. The interface is an asynchronous 8-bit data bus. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for M modules.

Control Logic

The control logic provides the electrical interface between the M-module bus and the module. The control registers are contained within this logic. The control logic also monitors the PPS output and indicates when a valid 1PPS or 100PPS output signal is available (PPSACT). Status is directly is available through an M-module register and an interrupt can be generated on any change.

Front Panel Connectors

The M1714 has four 68-pin front-panel connectors, labeled J200 and J203. See **Figure 7-2** for front panel connector locations. **Table 7-1** shows the signal assignments to connector pins.

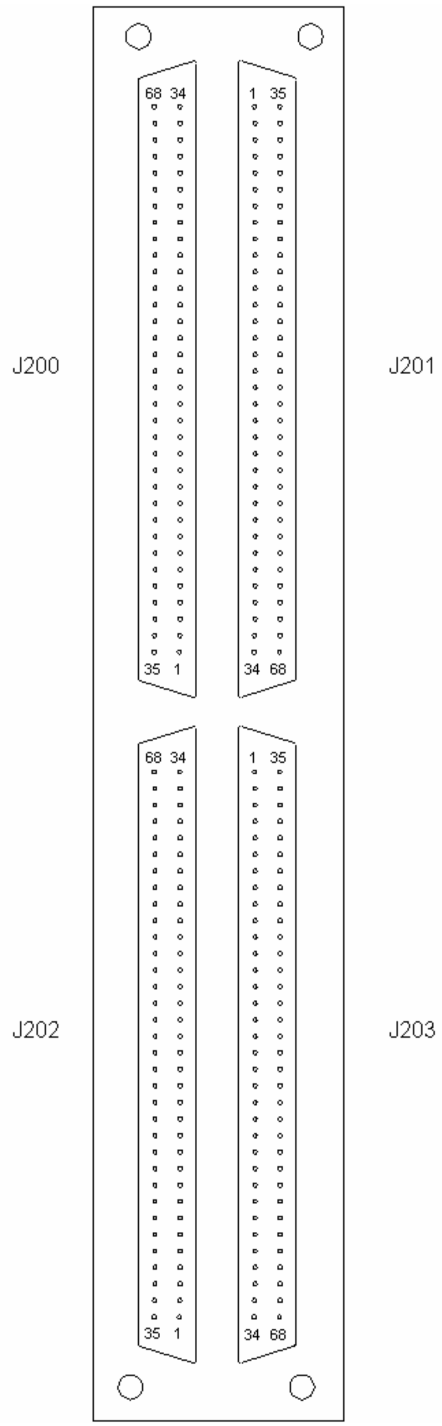

Figure 7-2 M1714 Front Panel Connectors

Table 7-1 M1714 Front Panel Pin-outs

J200			
68	GND	34	GND
67	1D0	33	GND
66	1D1	32	GND
65	1D2	31	GND
64	1D3	30	GND
63	1D4	29	GND
62	1D5	28	GND
61	1D6	27	GND
60	1D7	26	GND
59	2D0	25	GND
58	2D1	24	GND
57	2D2	23	GND
56	2D3	22	GND
55	2D4	21	GND
54	2D5	20	GND
53	2D6	19	GND
52	2D7	18	GND
51	3D0	17	GND
50	3D1	16	GND
49	3D2	15	GND
48	3D3	14	GND
47	3D4	13	GND
46	3D5	12	GND
45	3D6	11	GND
44	3D7	10	GND
43	4D0	9	GND
42	4D1	8	GND
41	4D2	7	GND
40	4D3	6	GND
39	4D4	5	GND
38	4D5	4	GND
37	4D6	3	GND
36	4D7	2	GND
35	GND	1	GND

J201			
1	GND	35	GND
2	GND	36	5D0
3	GND	37	5D1
4	GND	38	5D2
5	GND	39	5D3
6	GND	40	5D4
7	GND	41	5D5
8	GND	42	5D6
9	GND	43	5D7
10	GND	44	6D0
11	GND	45	6D1
12	GND	46	6D2
13	GND	47	6D3
14	GND	48	6D4
15	GND	49	6D5
16	GND	50	6D6
17	GND	51	6D7
18	GND	52	7D0
19	GND	53	7D1
20	GND	54	7D2
21	GND	55	7D3
22	GND	56	7D4
23	GND	57	7D5
24	GND	58	7D6
25	GND	59	7D7
26	GND	60	8D0
27	GND	61	8D1
28	GND	62	8D2
29	GND	63	8D3
30	GND	64	8D4
31	GND	65	8D5
32	GND	66	8D6
33	GND	67	8D7
34	GND	68	GND

J202			
68	GND	34	GND
67	9D0	33	GND
66	9D1	32	GND
65	9D2	31	GND
64	9D3	30	GND
63	9D4	29	GND
62	9D5	28	GND
61	9D6	27	GND
60	9D7	26	GND
59	10D0	25	GND
58	10D1	24	GND
57	10D2	23	GND
56	10D3	22	GND
55	10D4	21	GND
54	10D5	20	GND
53	10D6	19	GND
52	10D7	18	GND
51	11D0	17	GND
50	11D1	16	GND
49	11D2	15	GND
48	11D3	14	GND
47	11D4	13	GND
46	11D5	12	GND
45	11D6	11	GND
44	11D7	10	GND
43	12D0	9	GND
42	12D1	8	GND
41	12D2	7	GND
40	12D3	6	GND
39	12D4	5	GND
38	12D5	4	GND
37	12D6	3	GND
36	12D7	2	GND
35	GND	1	GND

J203			
1	GND	35	GND
2	GND	36	13D0
3	GND	37	13D1
4	GND	38	13D2
5	GND	39	13D3
6	GND	40	13D4
7	GND	41	13D5
8	GND	42	13D6
9	GND	43	13D7
10	GND	44	14D0
11	GND	45	14D1
12	GND	46	14D2
13	GND	47	14D3
14	GND	48	14D4
15	GND	49	14D5
16	GND	50	14D6
17	GND	51	14D7
18	GND	52	15D0
19	GND	53	15D1
20	GND	54	15D2
21	GND	55	15D3
22	GND	56	15D4
23	GND	57	15D5
24	GND	58	15D6
25	GND	59	15D7
26	GND	60	16D0
27	GND	61	16D1
28	GND	62	16D2
29	GND	63	16D3
30	GND	64	16D4
31	GND	65	16D5
32	GND	66	16D6
33	GND	67	16D7
34	GND	68	GND

Mating Connectors

The front panel connectors are a double VHDCI SCSI type of connector. **Table 7-2** contains manufacture's part numbers for the cable/connector assemblies used by the M1714.

Table 7-2 Mating Connectors

Manufacture	68 Pin Mating Cable
DDK Cable Assembly	DFG-HA2-XXX
Molex Connector	73796-3005
Molex Cable Assembly	92904-0001

Note- XXX represents length of cable

OPERATING MODE

The M1714 is a register-based module that is controlled through a series of I/O registers. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier.

There are a variety of registers used to configure and control the M1714 module. These registers are located in the I/O addressing space. The address map of the registers is shown in **Table 7-3**. Details of the registers are provided in the register definition section.

Table 7-3 M1714 Register Address Offset Assignments

Address Offset	Write	Read
00	---	M1714 Identity
02	---	M1714 Revision
04	BIST Command Register	BIST Status Register
06	*Reserved*	*Reserved*
08	*Reserved*	*Reserved*
0A	Direction Control Reg. for Octets 1-8	Direction Control Reg. for Octets 1-8
0C	Direction Control Reg. for Octets 9-16	Direction Control Reg. for Octets 9-16
0E	Master Write Strobe for Stimulus Data	Master Read Strobe for Response Data
10	Octet 1 Stimulus Data Register	Octet 1 Response Data Register
12	Octet 2 Stimulus Data Register	Octet 2 Response Data Register
14	Octet 3 Stimulus Data Register	Octet 3 Response Data Register
16	Octet 4 Stimulus Data Register	Octet 4 Response Data Register
18	Octet 5 Stimulus Data Register	Octet 5 Response Data Register
1A	Octet 6 Stimulus Data Register	Octet 6 Response Data Register
1C	Octet 7 Stimulus Data Register	Octet 7 Response Data Register
1E	Octet 8 Stimulus Data Register	Octet 8 Response Data Register
20	Octet 9 Stimulus Data Register	Octet 9 Response Data Register
22	Octet 10 Stimulus Data Register	Octet 10 Response Data Register
24	Octet 11 Stimulus Data Register	Octet 11 Response Data Register
26	Octet 12 Stimulus Data Register	Octet 12 Response Data Register
28	Octet 13 Stimulus Data Register	Octet 13 Response Data Register
2A	Octet 14 Stimulus Data Register	Octet 14 Response Data Register
2C	Octet 15 Stimulus Data Register	Octet 15 Response Data Register
2E	Octet 16 Stimulus Data Register	Octet 16 Response Data Register

Register Definitions

The following sections described the register and bit definitions that are contained within the M1714.

M1714 ID Register (00h)

This 8-bit read-only register identifies the M-module as a M1714 module. The value assigned to M1714 is “9C”h and is hard-wired inside the CPLD core.

Revision ID Register (02h)

This 8-bit read-only register contains a value that defines the revision number of the M1714. Initially this value is set to “01”h. If a revision change has been made to either the M1714 PCB or CPLD, this value will be incremented.

BIST Command Register (04h)

This register provides basic control over the device’s BIST functions. Only bits 1 and 0 are currently defined in this 8-bit register. Bits 7 through 2 are reserved for future use. After reset, all bits in this register are set to zero. **Figure 7-2** and **Table 7-4** describe these bits and how they should be set for operation of the M1714.

Figure 7-3 Command Register Bit Assignment for the M1714

BIST Command Register							
Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
X	X	X	X	X	X	Reset BIST ‘Fail’	Initiate BIST Cycle

Table 7-4 BIST Command Register Bit Definitions

Bit	Function
0	Initiate BIST Cycle **When set to ‘1’ initiates a BIST cycle. The BIST “Busy’ flag will be set in the status register.** Set to ‘0’ after reset.
1	Reset BIST ‘Fail’ **A value of ‘1’ resets the BIST ‘Fail’ flag in the status register. Set to ‘0’ after reset.**
7-2	Reserved

Status Register (04h)

This register tracks the status of the M1714 BIST. Only bits 1 and 0 are currently defined in this 8-bit register. Bits 7 through 2 are reserved for future use and are set to '0'. **Figure 7-4** and **Table 7-5** describe these bits.

Figure 7-4 BIST Status Register Bit Assignment for the M1714

BIST Status Register							
Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
X	X	X	X	X	X	BIST 'Fail'	BIST 'Busy'

Table 7-5 BIST Status Register Bit Definitions

Bit	Function
0	BIST 'Busy' A value of '1' indicates that the M1714 is performing a BIST cycle. This flag will be set to '0' upon the completion of the BIST cycle. Set to '0' after reset.
1	BIST 'Fail' **A value of '1' indicates that a failure has been detected during the BIST cycle. This bit is reset by writing a '1' to bit 1 of the Command register. Set to '0' after reset.**
7-2	Reserved

Direction Control for Octets 1-8 (0Ah)

This is a read/write register that controls the direction of the corresponding byte (octet). All eight channels within the octet will have the same direction. Writing a '1' to this register will set the appropriate octet to an output (stimulus.) A '0' value will set the octet to an input (response.) This register is set to '0' after reset. **Figure 7-5** describes this register.

Figure 7-5 Direction Control for Octets 1-8

Direction Control Reg. for Octets 1-8							
Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
Octet 8	Octet 7	Octet 6	Octet 5	Octet 4	Octet 3	Octet 2	Octet 1

Direction Control for Octets 9-16 (0Ch)

This is a read/write register that controls the direction of the corresponding byte (octet). All eight channels within the octet will have the same direction. Writing a '1' to this register will set the appropriate octet to an output (stimulus.) A '0' value will set the octet to an input (response.) This register is set to '0' after reset. **Figure 7-6** describes this register.

Figure 7-6 Direction Control for Octets 9-16

Direction Control Reg. for Octets 1-8							
Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
Octet 16	Octet 15	Octet 14	Octet 13	Octet 12	Octet 11	Octet 10	Octet 9

Master Write Strobe for Stimulus Data (0Eh)

A write to this address location causes a master write strobe to occur. A master write strobe loads the data in each octet stimulus holding register into the main output registers. This allows all 128 channels to change at once. Only octets that have been previously defined as outputs get written into the main output registers. The master write strobe is prohibited for main output registers whose octets have been programmed as inputs. Before a master write is issued, the octet stimulus holding registers that are defined as outputs, need to be loaded with the data that is to be written to the main output registers.

Master Read Strobe for Response Data (0Eh)

A read from this address location causes a master read strobe to occur. A master read strobe loads the data from all 128 channels into each octet response holding register. Data is written into the octet response holding register even if it has been previously defined as an output. It is up to software to determine which octet has valid input data. For octets that have been defined as outputs, the octet response holding register contains the output data.

Octet Stimulus / Response Data Register (10h – 2Eh)

A write to this register loads the stimulus data into the octet stimulus holding register. All octets that have been defined as outputs should have stimulus data loaded into their corresponding stimulus holding registers before a master write is performed. A read from this register reads the response data that was captured into the corresponding octet response holding register by a master read strobe.

Chapter 8
PRODUCT SUPPORT

Product Support

Racal Instruments has a complete Service and Parts Department. If you need technical assistance or should it be necessary to return your product for repair or calibration, call 1-800-722-3262. If parts are required to repair the product at your facility, call 1-949-859-8999 and ask for the Parts Department.

When sending your instrument in for repair, complete the form in the back of this manual.

For worldwide support and the office closes to your facility, refer to the Support Offices section on the following page.

Reshipment Instructions

Use the original packing material when returning the 3352 to Racal Instruments for calibration or servicing. The original shipping container and associated packaging material will provide the necessary protection for safe reshipment.

If the original packing material is unavailable, contact Racal Instruments Customer Service for information.

Support Offices

RACAL INSTRUMENTS

United States

(Corporate Headquarters and Service Center)
4 Goodyear Street, Irvine, CA 92618
Tel: (800) 722-2528, (949) 859-8999; Fax: (949) 859-7139

5730 Northwest Parkway Suite 700, San Antonio, TX 78249
Tel: (210) 699-6799; Fax: (210) 699-8857

Europe

(European Headquarters and Service Center)
18 Avenue Dutartre, 78150 LeChesnay, France
Tel: +33 (0)1 39 23 22 22; Fax: +33 (0)1 39 23 22 25

29-31 Cobham Road, Wimborne, Dorset BH21 7PF, United Kingdom
Tel: +44 (0) 1202 872800; Fax: +44 (0) 1202 870810

Via Milazzo 25, 20092 Cinisello B, Milan, Italy
Tel: +39 (0)2 6123 901; Fax: +39 (0)2 6129 3606

Racal Instruments Group Limited, Technologie Park,
D-51429 Bergisch Gladbach, Germany
Tel: +49 2204 844205; Fax: +49 2204 844219

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Instruments Repair Facility.

Model____________________Serial No.__________________________Date_____________

Company Name____________________Purchase Order #____________________________

Billing Address____
City

____
State/Province Zip/Postal Code Country

Shipping Address____
City

____
State/Province Zip/Postal Code Country

Technical Contact___________________________Phone Number (   )_________________
Purchasing Contact__________________________Phone Number (   )_________________

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

____
____
____
____

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type

____
____
____
____

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

____
____
____
____

4. Is calibration data required? Yes No (please circle one)

Call before shipping Ship instruments to nearest support office.

Note: We do not accept "collect" shipments.

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APPENDICES

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APPENDIX A – VX405C (P1 & P2) CONNECTORS

PIN	C	B	A
1	D08	-	D00
2	D09	-	D01
3	D10	-	D02
4	D11	BG0IN*	D03
5	D12	BG0OUT*	D04
6	D13	BG1IN*	D05
7	D14	BG10UT*	D06
8	D15	BG2IN*	D07
9	GND	BG20UT*	GND
10	SYSFAIL*	BG3IN*	-
11	-	BG3OUT*	-
12	SYSRESET*	-	DS1*
13	LWORD*	-	DS0*
14	AM5	-	WRITE*
15	A23	-	-
16	A22	AM0	DTACK*
17	A21	AM1	_
18	A20	AM2	_
19	A19	AM3	_
20	A18	GND	IACK*
21	A17	-	IACKIN*
22	A16	-	IACKOUT*
23	A15	GND	AM4
24	A14	IRQ7*	A07
25	A13	IRQ6*	A06
26	A12	IRQ5*	A05
27	A11	IRQ4*	A04
28	A10	IRQ3*	A03
29	A09	IRQ2*	A02
30	A08	IRQ1*	A01
31	+12 V	-	-12 V
32	+5 V	+5 V	+5 V

Figure A-1 P1 Pin Configuration

PIN	C	B	A
1	-	+5V	-
2	-	GND	-
3	GND	-	-
4	-	A24	GND
5	-	A25	-
6	-	A26	-
7	GND	A27	-
8	-	A28	-
9	-	A29	-
10	GND	A30	GND
11	-	A31	-
12	-	GND	-
13	-	+5V	-
14	-	D16	-
15	-	D17	-
16	GND	D18	GND
17	-	D19	-
18	-	D20	-
19	-	D21	-
20	-	D22	-
21	-	D23	-
22	GND	GND	GND
23	TTLTRG1*	D24	TTLTRG0*
24	TTLTRG3*	D25	TTLTRG2*
25	GND	D26	+5V
26	TTLTRG5*	D27	TTLTRG4*
27	TTLTRG7*	D28	TTLTRG6*
28	GND	D29	GND
29	-	D30	-
30	GND	D31	MODID
31	-	GND	GND
32	-	+5V	-

Figure A-2 P2 Pin Configuration

APPENDIX B: M213 CONNECTORS

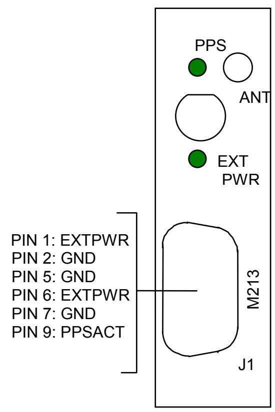

Figure B-1 M213 Front Panel I/O Signals

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure B-2 M213 M/MA Interface Connector Configuration

APPENDIX C: M212 CONNECTORS

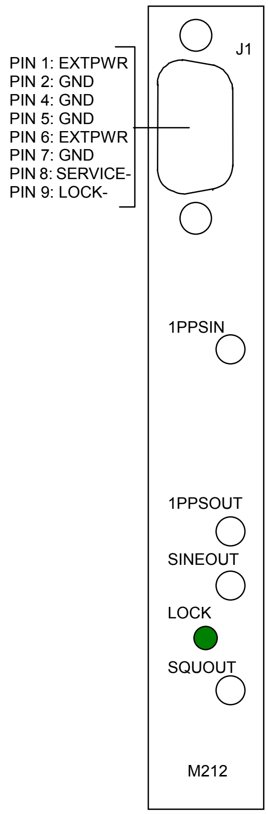

Figure C-1 M212 Front Panel I/O Signals

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure C-2 M212 M/MA Interface Connector Configuration

APPENDIX D: M1708 CONNECTORS

A high density DB15 female output connector supplies eight Square Wave copies of the 10 MHz TTL input (labeled PPS). Following is the pin-out for this connector:

Pin 1 Out1
Pin 2 Out2
Pin 3 Out3
Pin 4 Out4
Pin 5 Out5
Pin 6 Gnd
Pin 7 Gnd
Pin 8 Gnd
Pin 9 Gnd
Pin 10 Gnd
Pin 11 Out6
Pin 12 Out7
Pin 13 Out8
Pin 14 Gnd
Pin 15 Gnd

Two front panel SMB female connectors supply copies of the 10 MHz sine wave input.

Connector JA1 provides the connections for all signals between the 1708 M-Module and the host M-Module carrier board. The following signals are connected and used.

Pin #	Signal	Pin #	Signal
JA1-A1	/Chip_select	JA1-B1	GND
JA1-A8	Addr7	JA1-B2	VCC
JA1-A18	/DTACK	JA1-B3	+12V
JA1-A20	/RESET	JA1-B4	-12V
		JA1-B8	GND
		JA1-B9	D00
		JA1-B10	D01
		JA1-B11	D02
		JA1-B12	D03
		JA1-B13	D04
		JA1-B14	D05
		JA1-B15	D06
		JA1-B16	D07
		JA1-B17	/DSO
		JA1-B18	/WRITE
		JA1-B20	SYSCLOCK

Figure D-1 M1708 Connectors

APPENDIX E: M210 CONNECTORS

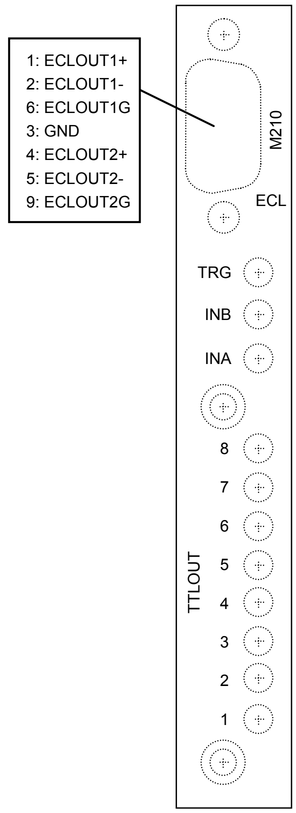

Figure E-1 M210 Front Panel Connector

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure E-2 M210 M-Module Interface